DAP 3200a Manual

Installation Guide and
Connector Reference

Version 1.10

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Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 3200a is high-performance Data Acquisition Processor suitable for high-speed data acquisition and control.

Features of the DAP 3200a:

- Intel 486 CPU
- 100 ns TIME resolution
- 769K samples per second
- ±2.5 volt, ±5 volt, 0-5 volt, and ±10 volt analog input ranges
- ±2.5 volt, ±5 volt, 0-5 volt, 0-10 volt, and ±10 volt analog output ranges

The onboard operating system for the DAP 3200a is DAPL 2000, which is optimized for 32-bit operation. The DAP 3200a also is compatible with DAPL version 4.

About This Manual

This manual includes hardware and software installation instructions and a hardware connector reference. Three other manuals provide information about creating data acquisition applications:

- The DAPL Manual contains a complete DAPL reference.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications.
- The Systems Manual describes support software that runs in the PC, including support for writing programs that run in the PC.

2. Installation, Testing, & Troubleshooting

Installing a Data Acquisition Processor involves the following steps:

1. If necessary, change jumper settings on the Data Acquisition Processor.
2. Install the Data Acquisition Processor.
3. Install the DAP Software.
4. Test the Installation.

Installation instructions are provided in this chapter. Advanced installation information is provided in Chapter 3. If there are any problems with installation, please read the troubleshooting guide at the end of this chapter.

Data Acquisition Processor Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge because it contains many high-speed analog and digital components. To protect the Data Acquisition Processor, observe the following precautions:

- Wear a grounding strap when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC offers protection.
- If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

System Requirements

The Data Acquisition Processor is compatible with 16-bit ISA or 32-bit EISA slots in AT/386/486/Pentium computers and requires version 3.0 or higher of DOS.

Standard Configurations

The Data Acquisition Processor is factory-configured to use interrupt 2 and I/O addresses in the range 220-22F (hexadecimal). This configuration does not conflict with most standard PC hardware. If you have nonstandard PC hardware or if any installed cards that use the same interrupt vector or I/O address as the Data Acquisition Processor, please read Chapter 3 before preceding with installation.

Note: Some sound cards are known to use I/O addresses in the 220-22F range. If your system has a sound card, check the configurations.

Interrupt and I/O address conflicts may cause subtle or obvious problems in your PC. After installing the Data Acquisition Processor, if your PC does not operate properly, check that there are no configuration conflicts.

Cooling Space Requirement

The DAP 3200a/214, DAP 3200a/315 and DAP 3200a/415 use clock-doubled or clock-tripled processors that require heat sinks for cooling. The DAP 3200a/315 uses a tall heat sink that takes up the space of two expansion slots. Consequently, a full-length expansion card can not be installed in the slot adjacent to the DAP 3200a/315 in the computer, although a half-card will fit. This large heat sink is required in systems with low air flow around the Data Acquisition Processor. For systems with sufficient air flow, an optional short heat sink that allows an expansion card to be installed in the adjacent slot is available from Microstar Laboratories. With an expansion card installed in the adjacent slot, the user must make sure there is an air flow of at least 400 linear feet per minute over the heat sink to guarantee adequate cooling.

Caution: Insufficient air flow can damage the Data Acquisition Processor.

The DAP 3200a/415 and DAP 3200a/214 use short heat sinks that allow a full-length expansion card to be installed in the adjacent slot.

Installing the Data Acquisition Processor

Caution: Do not install the Data Acquisition Processor while the PC is on.

To Install the Data Acquisition Processor:

1. Make any necessary changes to the hardware settings. Interrupt vector and I/O address information is provided in Chapter 3. Chapter 4 provides information about setting other hardware options. The default hardware settings are correct for msot systems.
2. Turn off the PC and remove the PC's cover.
3. Insert the Data Acquisition Processor into any free slot.

The Data Acquisition Processor requires approximately 15 Watts from the PC's power supply. If your system behaves erratically with the Data Acquisition Processor installed, the PC may need a larger power supply.

Installing DAP Software

Before installing the DAP Software, make backup copies of the diskette(s). Put the originals in a safe place, and use the backup disks for installation.

To Install Data Acquisition Processor Software:

1. Install the Data Acquisition Processor, as previously described.
2. Insert the DAP software disk into the PC's diskette drive.
3. At the DOS prompt, type `A:/INSTALL`.
4. Follow the on-screen instructions.

INSTALL prompts for configuration information including Data Acquisition Processor type and software destination directories. INSTALL provides information about each step to guide you through the installation process and provides options for copying DAPview and other software and Data Acquisition Processor support software to your PC.

INSTALL copies several files to your boot disk and adds information to your system configuration files `CONFIG.SYS` and `AUTOEXEC.BAT`. Backup copies of these files are created with the `.BAK` extension so that the original versions can be recovered.

Testing Installation

After running the INSTALL program, verify that software installation was successful by rebooting your PC. Before you see the DOS prompt, the following lines should appear on your screen:

```
ACCEL device driver 4.3
ACCEL driver initialization completed
DAPL initialization completed
```

The exact lines may vary slightly, depending upon configuration options. If a line is missing or if an error message appears, see the Troubleshooting section in this chapter.

When the DOS prompt is displayed, set the current directory to your DAPview directory and run DAPview by entering the following command:

```
DV
```

DAPview allows you to communicate interactively with the Data Acquisition Processor. Now everything you type at the PC keyboard is sent to the Data Acquisition Processor and all Data Acquisition Processor messages are printed on your screen. When the DAPview program begins, the following lines should be displayed on your screen:

```
*** DAPview [1.2] ***
*** DAPL Interpreter [4.XX XX/X] Serial# XXXXX ***
#
```

The appearance of the # prompt indicates that the Data Acquisition Processor is installed correctly. If the # prompt does not appear or if DAPview issues an error message and terminates, you have not established communication with the Data Acquisition Processor. Turn to the end of this chapter for troubleshooting hints.

Note: To exit from DAPview, press the Ctrl and Z keys simultaneously.

The number sign (#) indicates that the Data Acquisition Processor is waiting for a command. At this time you can enter DAPL commands from the keyboard or load DAPL command files. Sample applications are provided in the Applications Manual. The Systems Manual contains more information about DAPview.

Troubleshooting

The Systems Manual contains a list of the error messages which may be printed during software installation and system boot. The following errors commonly result from installation problems:

`INSTALL prints an error message.`
Find the error message in the “System Messages” chapter of the Systems Manual.

`At system startup, the “ACCEL device driver 4.3” message is not printed. OR DAPview prints the error message “Host communication port is uninitialized”`
Check that the file `CONFIG.SYS` is present on your boot volume. If this file was not present before installation, it should have been placed on your boot volume by INSTALL. If the file `CONFIG.SYS` is present, check that it includes the line

```
DEVICE=x:\yyy\ACOM.SYS ...
```

The `“x”` character should be the letter of your boot disk. `“yyy”` should be the correct directory where the file `ACOM.SYS` is located. If `CONFIG.SYS` is not on your boot volume, or if the `ACOM.SYS` line of the file `CONFIG.SYS` is incorrect, use INSTALL again, being careful to install the software on the correct volume.

`The message “Bad or missing ACOM.SYS” is printed.`
The file `ACOM.SYS` probably was not copied by INSTALL from the Data Acquisition Processor diskette to your boot volume. Use INSTALL again, being careful to install the software on the correct volume.

`When your system is booted, one of the following messages is printed:`

```
DAP hardware not found or improperly configured
DAP interrupt conflict
DAP interrupt selection error
```

These messages suggest a hardware conflict with another card in the PC; one or more of the Data Acquisition Processor configuration jumpers may need to be changed to resolve the conflict. See Chapter 3.

`At system startup, the message “ACCEL driver initialization completed” is not printed.`

If an error message is printed by the ACOMINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command ACOMINIT. If no ACOMINIT line is found, use INSTALL again, being careful to install the software on the correct volume.

`At system startup, the message “DAPL initialization completed” is not printed.`

If an error message is printed by the DAPLINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command DAPLINIT. If no DAPLINIT line is found, use the INSTALL pro-gram again, being careful to install the software on the correct volume.

`DAPview issues the error message “Could not establish communi-cations” OR DAPview does not display a DAPL # prompt.`

The Data Acquisition Processor is not communicating with your PC. This may indicate that an error occurred at boot time. Check that no error messages are printed when you boot your system.

If your PC has cards other than those listed at the beginning of the chapter, a card may be interfering with communications. Remove optional cards, boot the PC, and try using DAPview again.

Check that the configuration jumpers on the Data Acquisition Processor are correct. See Chapter 3 for the correct jumper selections. Check also for consistency between the jumper settings and the settings on the `ACOM.SYS` line in the file `CONFIG.SYS`.

A final possibility is that the Data Acquisition Processor may be faulty. If you suspect that this is the case, call Microstar Laboratories. When calling for installation support, please open your PC case so that the Data Acquisition Processor jumpers are visible, and be ready to provide the following information:

- the serial and model numbers of your Data Acquisition Processor.
- the contents of your `AUTOEXEC.BAT` and `CONFIG.SYS` files.
- a list of all hardware boards installed in your computer.

Your PC keyboard locks up when DAPview is started and does not accept the Ctrl-Z key.

Your PC may have an old style keyboard. Try starting DAPview with one of the following command line options:

```
DV /K1
DV /K2
```

DAPview issues the error “Help file DV.HLP not found.”

Check that the file DV.HLP has been copied to the directory containing the DAPview files. Check also to make sure the file AUTOEXEC.BAT has the line:

```
SET DV=C:\DV
```

Replace C:\DV with the drive and directory containing the DV.HLP file.

3. Advanced Installation Options

Installation for standard hardware configurations is described in Chapter 2. This chapter covers installation in more detail.

Nonstandard Configurations

The Data Acquisition Processor uses two resources from the host PC:

- an interrupt vector
- a range of I/O addresses

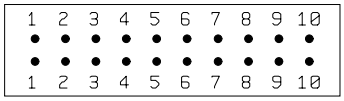
The Data Acquisition Processor allows several interrupt vector and I/O address selections. The interrupt vector may be 2, 3, 4, 5, 11, or 15. When selecting an interrupt vector, note the following interrupt vectors used by standard cards:

EGA/VGA	2
serial port COM2	3
serial port COM1	4
parallel port #2	5
hard disk controller on IBM XT	5
parallel port #1	7
secondary IDE controller	15

The Data Acquisition Processor is shipped configured to use interrupt 2. EGA and VGA video adapters potentially can use interrupt 2, but most applications do not use this capability. Since interrupt 2 does not conflict with any other standard hardware, this is the default Data Acquisition Processor interrupt vector.

If any other cards are installed, determine the interrupts used and select a Data Acquisition Processor interrupt number distinct from these. Depending on the selection, the host computer may lose access to one of the serial COM ports or one of the parallel ports.

To change interrupt vectors, locate the 20-pin `HOST CONFIGURE` connector:



J10 HOST CONFIGURE

Connector J10 is directly above the gold fingers on the Data Acquisition Processor printed circuit board.

There are six possible interrupt selections:

Interrupt Vector	Jumper
2	pin pair 9
3	pin pair 6
4	pin pair 7
5	pin pair 8
11	pin pair 5
15	pin pair 4

To change the interrupt, remove the jumper and replace it according to this table. Note that exactly one of the pin pairs 4, 5, 6, 7, 8, and 9 should be connected.

When the interrupt is changed, the INSTALL program must be informed of the new interrupt selection. When running INSTALL, select the DAP 0 button and select the interrupt number that matches the interrupt of the Data Acquisition Processor.

In addition to an interrupt vector, the Data Acquisition Processor uses a range of I/O addresses. If a sound card or any nonstandard cards are used in the host PC, check that the Data Acquisition Processor I/O addresses do not conflict with those cards.

The Data Acquisition Processor is shipped configured to use I/O addresses in the range 220-22F (hexadecimal). This range may be changed by changing the jumpers on the HOST CONFIGURE connector. Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1, 2, 3
230 - 23F	2, 3
240 - 24F	1, 3
250 - 25F	3
320 - 32F	1, 2
330 - 33F	2
340 - 34F	1

When the I/O address is changed, the INSTALL program must be informed of the new address selection. When running INSTALL, select the DAP 0 button and select the address that matches the address of the Data Acquisition Processor.

Note: The only effect of changing the interrupt number or address in the INSTALL program is to change the value of the /I or /A parameter of the line ACOM.SYS that is inserted in the file CONFIG.SYS.

The INSTALL Program

This section provides additional details about the INSTALL program. This information is of interest only to advanced Data Acquisition Processor users.

The INSTALL program installs Data Acquisition Processor software on a PC and configures the PC to initialize the ACCEL driver when the PC boots. INSTALL uses the following syntax:

```
A: INSTALL <options>
```

If installing from a drive other than A:, type the letter for that drive instead. INSTALL allows several command line options for special installation features. The following options are legal:

/COMx	Use serial port communication on com port x (DAP 801 only)
/Mxx	Default ACCEL driver mode (See the Systems Manual)
/Dx	Install more than one DAP
/?	Help

When running INSTALL, several prompts are provided for configuring Data Acquisition Processor software on a PC. Select a DAP button to choose the DAP model, address, and interrupt for the Data Acquisition Processor. Choose the "Select Software Options" button to select the specific software options to install. For help on the options press F1.

After all options have been verified, INSTALL copies Data Acquisition Processor software to the PC and modifies the system files. INSTALL copies the files ACOM.SYS, ACOMINIT.EXE, DAPLINIT, and Dx-x.STD to the PC boot drive. INSTALL creates the file ACOM.DAT and places it on the boot drive. These files are all placed on the boot drive so they are available when the PC first boots.

After copying the boot files, INSTALL copies the software that was specified in the Select Software Options dialog box to the Main directory.

INSTALL adds a line to the file CONFIG.SYS that loads the ACCEL device driver. If this line already exists from a previous installation, INSTALL replaces it. The following line is a typical line that INSTALL adds to CONFIG.SYS:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

More information about the ACCEL driver configuration line is provided later in this chapter. If CONFIG.SYS does not exist, INSTALL creates it. Before modifying CONFIG.SYS, INSTALL saves an original copy in the file CONFIG.BAK.

INSTALL also modifies the file AUTOEXEC.BAT by adding several lines that configure the ACCEL driver with specific communication information. If these lines already exist from a previous installation, INSTALL replaces them. The following lines are typical lines that INSTALL adds to AUTOEXEC.BAT:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

The ACOMINIT program configures the ACCEL driver with specific communication pipe information provided by the file ACOM.DAT. For some Data Acquisition Processor models, the DAPLINIT program is required to initialize the DAPL operating system. More information about the ACOMINIT and DAPLINIT programs is provided later in this chapter. If AUTOEXEC.BAT does not exist, INSTALL creates it. Before modifying AUTOEXEC.BAT, INSTALL saves an original copy in the file AUTOEXEC.BAK.

Device Driver Configuration

This section explains the format of the device driver command that is placed in the `CONFIG.SYS` file by the INSTALL program. This information is of interest only to advanced programmers.

The format of the device driver command is:

```
DEVICE=ACOM.SYS [Ix] [DAP[yyy]:Azzz] [Muu] [Pwww]
```

Note: Several parameters are optional. The letters u through z in each parameter represent hexadecimal digits.

`x` specifies the interrupt vector that is used for PC communication. This number should match the configuration of jumper `J10` on the Data Acquisition Processor.

The ACCEL driver automatically detects the type of Data Acquisition Processor that is installed. `yyy` is optional and manually specifies the board type. For the DAP 3200a, `yyy` is `3200a`.

`zzz` specifies the hexadecimal starting I/O address of the Data Acquisition Processor. This number must match the configuration of jumper `J10` on the Data Acquisition Processor.

`uu` is a hexadecimal number that specifies the default mode of the ACCEL driver. See the Systems Manual for more information about ACCEL driver modes.

`www` is a hexadecimal number that specifies the number of paragraphs of memory to reserve for PC communications pipes. See “Com Pipe Configuration” later in this chapter.

The following is a typical ACCEL driver command line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

The ACCEL driver can be loaded into high memory with the DOS `devicehigh` statement. See your DOS manual for details.

The ACOMINIT Program

ACOMINIT configures the ACCEL driver communication pipes. ACOMINIT is placed in the file `AUTOEXEC.BAT` to configure the ACCEL driver when the PC first boots. The syntax for ACOMINIT is:

```
ACOMINIT <cfg_file>
```

`<cfg_file>` provides communication pipe configuration information. `<cfg_file>` normally is named `ACOM.DAT`. The following section describes the contents of `ACOM.DAT`.

Com Pipe Configuration

This section describes the format of communication pipe configuration in the file `ACOM.DAT`. This information is not required for most applications. During initialization, the Microstar Laboratories program ACOMINIT reads the contents of a configuration file which specifies a com pipe configuration. The configuration file determines the connection between com pipes on the Data Acquisition Processor and com pipes on the PC. Lines in the configuration file have the following syntax:

```
<source> -> <destination> [<options>]
```

`<source>` and `<destination>` are specifications of communication pipe locations. A com pipe location is either a Data Acquisition Processor com pipe, a PC com pipe, or a PC serial port:

```
(DAP[n] CPIPE v)
(PC CPIPE w)
```

`n` is the Data Acquisition Processor number when several boards are installed in one PC. `v` is a DAPL com pipe number, `w` is a PC com pipe number. The space before `v` and `w` can be omitted.

For example, the following lines connect the default text input and text output com pipes of the Data Acquisition Processor to the PC:

```
(dap cpipe 0) -> (pc cpipe 0)
(pc cpipe 0) -> (dap cpipe 0)
```

The first line connects DAPL output com pipe 0 to PC input com pipe 0. The second line connects PC output com pipe 0 to DAPL input com pipe 0. By default, DAPL

defines two input com pipes and two output com pipes. Output com pipe 0, named $SYSOUT, is for text output to the PC. Output com pipe 1, named $BINOUT, is for binary output to the PC. Input com pipe 0, named $SYSIN, is for text input from the PC. Input com pipe 1, named $BININ, is for binary input from the PC.

Each line in the com pipe configuration file may contain one or more options, enclosed in square brackets. The following options are available:

```
BINARY|TEXT
MAXSIZE=xx
WIDTH BYTE | WORD | LONG
```

BINARY and TEXT specify the type of the data in the com pipe. The default is TEXT.

MAXSIZE specifies the size of the PC buffer of the com pipe, in bytes. The default is 1024 bytes. The INSTALL program sets the maximum size of the com pipes to be relatively small to conserve PC memory yet provide good performance. The Data Acquisition Processor automatically provides additional pipe buffering when needed. In some applications, increasing the maximum com pipe size can improve performance by allowing larger block operations. Performance can increase with com pipe sizes up to 4096 or 8192. Larger com pipe sizes typically do not provide further performance benefits.

WIDTH specifies the width of data items that are transferred through the com pipe. The WIDTH option must match the width of the corresponding Data Acquisition Processor com pipe. BYTE is the default for text com pipes and also is the only width allowed. WORD is the default for binary com pipes. Any width is allowed for binary com pipes.

The default com pipe configuration file generated by the INSTALL program is stored in the file ACOM.DAT. If the Data Acquisition Processor is operated inside a PC, the following configuration is placed in the file ACOM.DAT:

```
(dap0 cpipe0) -> (pc cpipe0) [text maxsize=1024]
(pc cpipe0) -> (dap0 cpipe0) [text maxsize=1024]
(dap0 cpipe1) -> (pc cpipe1) [binary maxsize=2048]
(pc cpipe1) -> (dap0 cpipe1) [binary maxsize=1024]
```

In some applications, additional com pipes need to be defined. More com pipes are needed when extra com pipes are defined in DAPL on a Data Acquisition Processor or when several Data Acquisition Processors are installed.

For special applications, extra com pipes can be defined in DAPL. See the CPIPE command in the DAPL Manual.

Note that in many cases, the commands `MERGE`, `MERGEF`, and `NMERGE` can be used instead of defining extra com pipes. It is best to use standard com pipes when possible to maintain a standard communication setup.

When more than one Data Acquisition Processor is installed in a system, additional com pipes need to be defined. For several Data Acquisition Processors, the following com pipe numbering is recommended:

```
DAP0
   system text pipe is PC com pipe #0
   system binary pipe is PC com pipe #1
DAP1
   system text pipe is PC com pipe #2
   system binary pipe is PC com pipe #3
 .
 .
DAP6
   system text pipe is PC com pipe #12
   system binary pipe is PC com pipe #13
```

P Parameter Size

In a system with additional com pipes, the memory available to the ACCEL driver must be increased. The `P` parameter in the `ACOM.SYS` line of the file `CONFIG.SYS` specifies the number of paragraphs of PC memory reserved for the ACCEL driver and com pipes. The storage requirement of the ACCEL driver and PC com pipes, in bytes, is:

```
storage = 830 + (maxsize in bytes) + (number of com
pipes)*190
```

`MaxSize in bytes` is the sum of all com pipe sizes defined in the file `ACOM.DAT`. `Number of com pipes` is the number of com pipes defined.

Note: This storage requirement applies for version 4.34 of the ACCEL driver. Subsequent driver versions may require additional storage.

The `P` parameter is a hexadecimal number, specified in paragraphs. A paragraph of PC memory is 16 bytes. To determine the `P` parameter, divide the storage requirements by 16 and convert to hexadecimal.

The following example calculates the `P` parameter for the default `ACOM.DAT` file created by INSTALL. The result, in bytes, is divided by 16 to get the `P` parameter in paragraphs.

```
storage = 830 + 5120 + 4*190 = 6710 bytes
p= 6710/16 = 420 paragraphs (decimal) = 1A4 (hex)
```

When defining additional com pipes, remember to define pipes for both the DAP-to-PC and PC-to-DAP direction. Some programs such as DAPview for Windows expect additional com pipes defined for both directions.

DAP-to-DAP Communication

Communication pipes can be configured to allow communication between two Data Acquisition Processors. DAP-to-DAP communication occurs over the PC bus in the background with no PC program intervention required. The following syntax is used in the file ACOM.DAT to configure DAP-to-DAP communication:

```
(DAPw CPIPEx) -> (DAPy CPIPEz)
(DAPy CPIPEz) -> (DAPw CPIPEx)
```

w is the number of the DAP that sends data. x is the DAP communication pipe used to send data. y is the number of the DAP that receives data. z is the DAP communication pipe to receive data. The DAPL command CPIPE is needed to define the DAP communication pipes on each DAP.

The following example shows how to configure a system for DAP-to-DAP communication. This example configures two DAPs. DAP 0 samples one channel of data and sends the data to DAP 1 for analog output.

In the file ACOM.DAT, add:

```
(dap0 cpipe15) -> (dap1 cpipe15)   [binary maxsize=1024]
(dap1 cpipe15) -> (dap0 cpipe15)   [binary maxsize=1024]
```

DAP-to-DAP com pipes require twice the storage space as DAP-to-PC or PC-to-DAP com pipes. For the above DAP-to-DAP com pipe definition, the P parameter in CONFIG.SYS must be increased by 130 (hex). The following example calculates the P-parameter increase:

```
storage increase= 2 * (2048 + 2 * 190) = 4856 (decimal)
p increase=4856/16 = 304 paragraphs (decimal) = 130 (hex)
```

The following DAPL commands provide an example of how to implement DAP-to-DAP communication.

```
;  DAPL commands for DAP 0:
CPIPE TODAP1 PC NUM=15 OUTPUT BINARY WORD
RESET
IDEF A 1
   SET IPIPE0 S0
   TIME 10000
   END
PDEF B
   COPY(IPIPE0, TODAP1)
   END
START A,B

;  DAPL commands for DAP 1:
CPIPE FROMDAP0 PC NUM=15 INPUT BINARY WORD
RESET
PDEF A
   COPY(FROMDAP0, $BINOUT)
   END
START A
```

The DAPLINIT Program

DAPLINIT initializes the DAPL operating system on the Data Acquisition Processor by downloading a binary image of DAPL to the Data Acquisition Processor. ACCEL driver communication pipes must be configured using ACOMINIT before DAPLINIT is run. The syntax for DAPLINIT is as follows:

```
DAPLINIT [/RESET] [<dapl_file>] [<dapl_file>]*
```

`<dapl_file>` specifies a binary file containing DAPL. DAPLINIT allows several DAPL binary files to initialize several Data Acquisition Processors in a PC.

The optional parameter `/RESET` requests a hardware reset of the Data Acquisition Processor before downloading DAPL. If `/RESET` is not specified, all Data Acquisition Processors retain their state during a warm PC boot.

DAPLINIT detects the Data Acquisition Processor model types on the `ACOM.SYS` line of the file `CONFIG.SYS`. DAPLINIT downloads the DAPL files, in order, to the Data Acquisition Processors that require DAPL initialization.

DAPLINIT can accept a wildcard file specification to allow flexibility for when DAP installations change. With a wildcard file name, DAPLINIT searches the current directory and the DOS PATH to find a DAPL binary file that matches the DAP type that is installed. The following example shows how DAPLINIT can be configured to search for the correct `DAPL/STANDARD` binary file.

```
DAPLINIT /RESET D*.STD
```

The INSTALL program automatically configures new installations to use a wildcard file name for DAPLINIT.

Installing Several Data Acquisition Processors

Up to seven Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. For special options to install up to 14 Data Acquisition Processor boards in one PC, contact Microstar Laboratories.

Each Data Acquisition Processor requires one PC slot. All the Data Acquisition Processors in a PC share just one interrupt line; no DMA lines are required. The Data Acquisition Processors are distinguished by their I/O addresses in the PC. Before installing Data Acquisition Processors in the PC, select a distinct I/O address for each board.

There are seven possible I/O addresses; this limits the number of Data Acquisition Processors in a PC to seven. Set the I/O addresses with the jumpers on the `HOST CONFIGURE` connector. Information about the `HOST CONFIGURE` connector is provided at the beginning of this chapter.

Note: Pin pair 10 of the `HOST CONFIGURE` connector, `J10`, sets the level of the PC's interrupt line. Pin pair 10 must be connected for one Data Acquisition Processor in a PC, and must not be connected for all other Data Acquisition Processors.

INSTALL can perform installation for several Data Acquisition Processors. When typing the INSTALL command, add the option `/Dx` to the end of the command, where `x` is the number of boards. For example, the following line defines installation for three Data Acquisition Processors.

```
A:INSTALL /D3
```

INSTALL provides on-screen options for configuring each Data Acquisition Processor individually. Select a `DAP` button to display a dialog box for choosing the Data Acquisition Processor model, address, and interrupt.

Note: The order in which the boards appear in the `ACOM.SYS` line in the file `CONFIG.SYS` determines the numbering of the Data Acquisition Processors. The first Data Acquisition Processor is `DAP 0`, the second is `DAP 1`, etc. The addresses do not matter when determining the numbering. When synchronous operation is used with DLOG, the last board in the list is the master unit.

Installation on a Network

Data Acquisition Processor software can be installed on a network consisting of PC workstations connected to one or more servers. The INSTALL program can copy Data Acquisition Processor software to a PC workstation from a network that has a copy of the DAP Software disk image.

Note: When using Data Acquisition Processor software on a network, each simultaneous user must have a licensed copy of the software.

When installing Data Acquisition Processor software from a network, INSTALL copies several files to the PC workstation boot drive. The files are `ACOM.SYS`, `ACOMINIT.EXE`, `ACOM.DAT`, and, if necessary, `DAPLINIT.EXE` and `Dx-x.STD`. These files must be on the PC boot drive so that they are available immediately at boot time. INSTALL copies the remaining Data Acquisition Processor software to a network drive for use once the network is connected. INSTALL modifies `AUTOEXEC.BAT` and `CONFIG.SYS` on the workstation boot drive as in regular installations.

DAPL Licensing

When a Data Acquisition Processor is shipped from the factory, a copy of DAPL is provided that is licensed to run on the Data Acquisition Processor. When a DAP Software Upgrade is shipped, the DAPL file on the upgrade is licensed to be used with the Data Acquisition Processor that was specified when the upgrade was ordered.

Removing Data Acquisition Processor Software

When a Data Acquisition Processor is removed from a PC, the software can be removed as well. This section describes how to remove a Data Acquisition Processor software installation.

1. Delete the directory where Data Acquisition Processor software was in-stalled. Usually this directory is `c:\dap`. Delete all the subdirectories under the DAP directory. Make sure that there are no important data files in these directories before deleting them.

2. Edit the file `AUTOEXEC.BAT`. Delete the following four lines:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

3. Edit the file `CONFIG.SYS`. Delete the following line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

4. DAP 3200a Connectors

This chapter discusses the interface connectors on the DAP 3200a. Diagrams and documentation for the analog input/output connector, the digital input/output connector, the output clock connector, and jumpers are provided in this chapter. Also included are detailed instructions for setting the following options:

- the analog input voltage range (J7, J8, J9 and J14)
- the output voltage ranges of DAC0 and DAC1 (J11 and J12)
- the digital output polarity at power-on (J32)
- input/output synchronization (J22)

Figure 1 shows component placement outlines of the DAP 3200a. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.

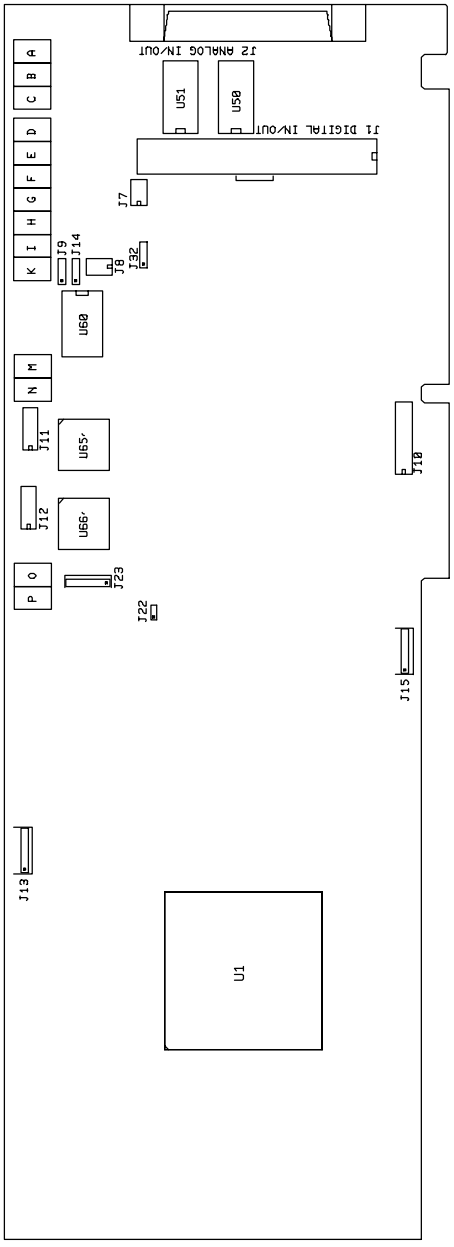


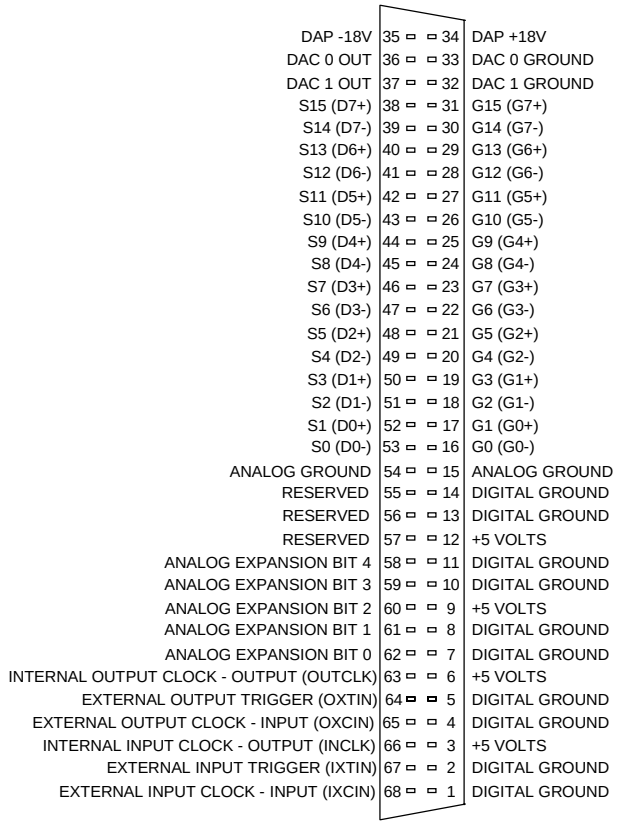
Figure 1.

DAP 3200a

Analog Input/Output Connector

Analog voltages are connected to the Data Acquisition Processor through a 68-pin connector on the back panel of the PC. This connector is located on the right side of the Data Acquisition Processor and is labeled `J2 ANALOG IN/OUT`. It has a double row of pins on 0.050 inch centers. The connector is 3M part number 10268-52E2VC or AMP part number 2-178238-8. It mates with discrete wire connector 3M part number 10168-6000EC or AMP 2-175677-8. Both connectors are shielded and are compatible with round cable. The analog I/O connector also mates with insulation displacement ribbon cable connector 3M part number 10168-8100EE. The insulation displacement connector is compatible with 0.025" pitch ribbon cable.

Looking at the analog connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended inputs are indicated by `S0` through `S15`; their corresponding ground inputs are `G0` through `G15`. Differential inputs are indicated by `D0-` and `D0+` through `D7-` and `D7+`; their corresponding ground inputs are `G0-` and `G0+` through `G7-` and `G7+`. Every differential signal must be referenced to the corresponding ground. Data Acquisition Processors have a limited common mode voltage range and a ground connection must be used to assure that this range is not exceeded.

A single-ended analog signal should be connected to an analog input pin and to an analog ground pin, for example to pins 53 and 16. A differential analog signal should be connected to two adjacent analog input pins and either of their corresponding grounds, for example to input pins 52, 53, and ground pin 16 or 17.

Termination boards to connect all lines of the analog connector to discrete wires are available from Microstar Laboratories.

The DAP 3200a features fault-protected input multiplexers. Fault protected input multiplexers allow signals to be connected to the Data Acquisition Processor with power off and allow a higher input voltage without damaging the inputs. Spare fault-protected input multiplexers are available from Microstar Laboratories.

Analog input signals should be within the range from -25 volts to +25 volts, relative to the ground of the Data Acquisition Processor. Input signals may be applied to the Data Acquisition Processor when the PC's power is off. See Chapter 5 for electrical characteristics of the analog input pins.

The analog I/O connector of the Data Acquisition Processor includes digital-to-analog converter output pins and analog supply voltages. Pins 36 and 37 are the outputs of `DAC0` and `DAC1`, respectively. Pins 33 and 32 are the grounds for `DAC0` and `DAC1`, respectively. The digital-to-analog converters have voltage outputs with typical output impedance of 0.05 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps, but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When `J32` is moved, the analog outputs at power-on may vary by up to 5 millivolts.

Pin 15 is analog power ground. Pins 34 and 35 are connected to +18 volt and -18 volt analog supplies. The maximum allowable current drain from these supplies is 20 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5-volt digital power supply found on the analog control connector with an external DC-to-DC converter.

The analog I/O connector also provides analog input expansion control lines, an external trigger input, an external input clock input, an internal input clock output, and connections to the 5-volt digital supply and its ground.

Pins 62-58 provide TTL-compatible analog input expansion control signals that select the expansion port. The five highest order bits of the input pin number appear in descending order on pins 58, 59, 60, 61, and 62 for a period starting one sample time before the analog input is sampled.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 32 differential inputs, or up to 64 single-ended inputs, or any combination requiring up to 64 input lines. A Data Acquisition Processor can control up to 8 external expansion boards, for a total of 512 input lines.

The analog I/O connector has an input pin for an active high external trigger. Sampling is inhibited if the external trigger is inactive when an input procedure is started. Sampling then commences on the inactive to active transition.

The external trigger is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger is ignored if there is no `HTRIGGER` command in the active input procedure. See Chapter 6 for more information.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

The analog I/O connector has input and output pins for an external input clock. The input pin should be used to connect an external input clock. The output pin is the buffered output of the internal clock circuit. See Chapter 6 for more information.

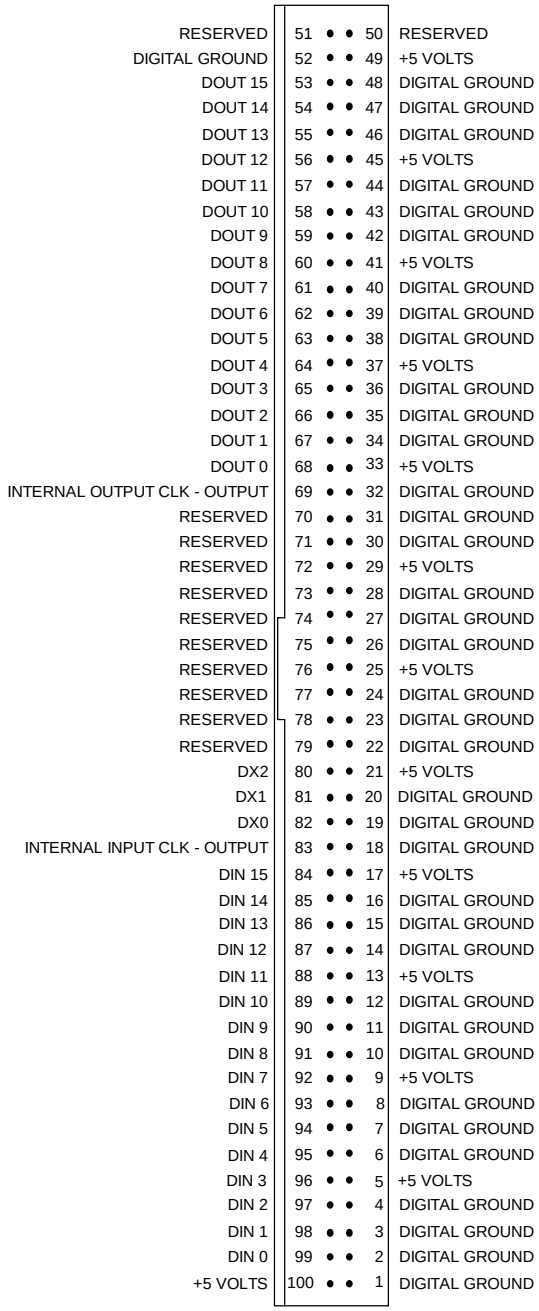
Pins 3, 6, 9, and 12 provide +5 volt power. Maximum current from the +5 volt supply is 1 Amp.

Digital Input/Output Connector

The digital input/output connector is a vertical 100-pin connector labeled `J1 DIGITAL IN/OUT`. This connector is near the right edge the Data Acquisition Processor, to the left of the analog input/output connector. The digital I/O connector has two rows of 50 pins on 0.050 inch centers. This connector is manufactured by AMP, part number 1-104549-0. The digital I/O connector mates with insulation displacement connector AMP 1-111196-6.

The digital I/O connector is not accessible from the back of the PC. A cable, part number MSCBL 042, that makes the digital connector accessible at the adjacent slot in the PC is available from Microstar Laboratories. For systems that comply with the European EMC Directive, MSCBL 046 provides the same functionality as MSCBL 042 but with a shielded connector. Contact Microstar Laboratories for more details.

The pin numbering of the digital input/output connector is shown in the following diagram:


RESERVED 51 50 RESERVED
DIGITAL GROUND 52 49 +5 VOLTS
DOUT 15 53 48 DIGITAL GROUND
DOUT 14 54 47 DIGITAL GROUND
DOUT 13 55 46 DIGITAL GROUND
DOUT 12 56 45 +5 VOLTS
DOUT 11 57 44 DIGITAL GROUND
DOUT 10 58 43 DIGITAL GROUND
DOUT 9 59 42 DIGITAL GROUND
DOUT 8 60 41 +5 VOLTS
DOUT 7 61 40 DIGITAL GROUND
DOUT 6 62 39 DIGITAL GROUND
DOUT 5 63 38 DIGITAL GROUND
DOUT 4 64 37 +5 VOLTS
DOUT 3 65 36 DIGITAL GROUND
DOUT 2 66 35 DIGITAL GROUND
DOUT 1 67 34 DIGITAL GROUND
DOUT 0 68 33 +5 VOLTS
INTERNAL OUTPUT CLK - OUTPUT 69 32 DIGITAL GROUND
RESERVED 70 31 DIGITAL GROUND
RESERVED 71 30 DIGITAL GROUND
RESERVED 72 29 +5 VOLTS
RESERVED 73 28 DIGITAL GROUND
RESERVED 74 27 DIGITAL GROUND
RESERVED 75 26 DIGITAL GROUND
RESERVED 76 25 +5 VOLTS
RESERVED 77 24 DIGITAL GROUND
RESERVED 78 23 DIGITAL GROUND
RESERVED 79 22 DIGITAL GROUND
DX2 80 21 +5 VOLTS
DX1 81 20 DIGITAL GROUND
DX0 82 19 DIGITAL GROUND
INTERNAL INPUT CLK - OUTPUT 83 18 DIGITAL GROUND
DIN 15 84 17 +5 VOLTS
DIN 14 85 16 DIGITAL GROUND
DIN 13 86 15 DIGITAL GROUND
DIN 12 87 14 DIGITAL GROUND
DIN 11 88 13 +5 VOLTS
DIN 10 89 12 DIGITAL GROUND
DIN 9 90 11 DIGITAL GROUND
DIN 8 91 10 DIGITAL GROUND
DIN 7 92 9 +5 VOLTS
DIN 6 93 8 DIGITAL GROUND
DIN 5 94 7 DIGITAL GROUND
DIN 4 95 6 DIGITAL GROUND
DIN 3 96 5 +5 VOLTS
DIN 2 97 4 DIGITAL GROUND
DIN 1 98 3 DIGITAL GROUND
DIN 0 99 2 DIGITAL GROUND
+5 VOLTS 100 1 DIGITAL GROUND

Pins 1 and 100 are closest to the gold edge fingers of the Data Acquisition Processor.

Digital inputs are indicated by `DIN 0-15` and digital outputs are indicated by `DOUT 0-15`. Bit 0 is the least significant bit.

A termination board from Microstar Laboratories, part number MSTB 008, connects all lines of the digital connector to discrete wire connectors.

The digital inputs are FCT TTL with 10K pull-up resistors. The digital inputs sink no more than 5 microamps for a “1” input and source no more than 0.5 milliamps for a “0” input. An input voltage greater than 2 V is interpreted as a “1” and an input voltage less than 0.8 V is interpreted as a “0”. When no signal is connected a digital input is read as a “1” due to the pull-up resistors.

Digital inputs may have TTL signals applied when the Data Acquisition Processor is off.

Digital output polarity at power-on is selected by `J32`, the Digital Output Reset Polarity Jumper, described later in this chapter.

The digital outputs are FCT TTL; they can sink no more than 12 milliamps for a “0” output and can source no more than 15 milliamps for a “1” output. The output voltage for a “1” is greater than 2.4 V and the output voltage for a “0” is less than 0.50 V.

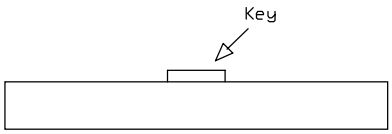
The digital input/output connector has multiple connections for the Data Acquisition Processor +5 V power supply. The supply current is rated at 500 milliamps per connection with a total current limit of 2 Amps. The 2 Amp current limit is due to the limited current available from the host computer.

Pins 80, 81, and 82 provide TTL-compatible digital input expansion control signals. The low-order bit of the port number appears on pin 82, the middle bit appears on pin 81, and the high-order bit appears on pin 80.

An optional digital input port may be specified in a DAPL `SET` command. The digital input port numbers range from 0 to 7. The specified port number appears on the control pins for a period starting one sample time before the time at which the digital inputs are sampled. The port number can be used to control external multiplexers.

An external digital expansion board is available from Microstar Laboratories. Each external expansion board allows up to 64 digital inputs and 64 digital outputs.

The Microstar Laboratories cable MSCBL 036-01 is compatible with the digital input/output connector. The diagram below shows the key on the cable. This key must be towards the left side of the Data Acquisition Processor.



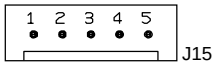
Note: Cables not made by Microstar Laboratories may have different keys.

Output Clock Connector

Connector `J15` is a five pin connector, Molex part number 22-23-2051; the mating connector is Molex part number 22-01-3057. `J15` is located on the lower edge of the Data Acquisition Processor, near the center of the board.

The output clock signals and the output trigger signal are on connector `J15`, along with power and ground. These signal pins can be used to control when outputs are updated. See Chapter 6 for more details.

The pin numbering for `J15` is given in the following table:



Pin 1	Ground
Pin 2	External output trigger — input
Pin 3	Internal output clock — output
Pin 4	External output clock — input
Pin 5	+5 volts

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. range amplifier
5. analog-to-digital converter with sample-and-hold amplifier

Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the range amplifier, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The range amplifier allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from three bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration

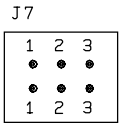
Four connectors control the analog signal path of the DAP 3200a. Note that changing voltage ranges may require recalibration.

The following table summarizes the DAP 3200a analog input jumper connections:

ADC Range	J7	J8	J9	J14
0 to 5 v	2	3	1 - 2	1 - 2
± 2.5v	1	2	2 - 3	1 - 2
± 5v*	2 *	3 *	2 - 3 *	1 - 2 *
± 10 v	2	3	2 - 3	2 - 3

* Factory Configuration

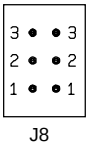
The input signal to the range amplifier is selected by J7.



Exactly one jumper should be placed on J7, as follows:

Jumper	Range amplifier input
1	range amplifier disabled
2	programmable gain amplifier
3	instrumentation amplifier

The input signal to the analog-to-digital converter is selected by J8.

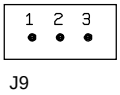


Exactly one jumper should be placed on J8, as follows:

Jumper	Analog-to-digital converter input
1	instrumentation amplifier
2	programmable gain amplifier
3	range amplifier

Note that jumpers on J8 are placed horizontally.

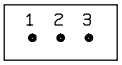
The signal range of the range amplifier is selected by J9 and J14. J9 selects between unipolar inputs and bipolar inputs.



One jumper should be placed on J9 as follows:

Jumper	Signal range
1-2	unipolar
2-3	bipolar

J14 selects the input signal range of the range amplifier.



J14

One jumper should be placed on J14 as follows:

Jumper	Input signal range
1-2	0 to 5 Volts
1-2	± 2.5 Volts
1-2	± 5 Volts
2-3	± 10 Volts

Note: Regardless of the input voltage range, positive and negative differential signals may range from -25 volts to +25 volts without damaging the Data Acquisition Processor.

Note: There is a maximum speed reduction for the ± 10-volt input range on the DAP 3200a. Using the input voltage range of ± 10 volts, the minimum TIME is 2.4 µs, which is approximately 417K samples/second.

Analog Output Voltage Range Selection

The voltage ranges of DAC0 and DAC1 are selected by headers J11 and J12, respectively:

Three or four jumpers should be placed on J11 and J12, as follows:

Jumpers	Range
2-3, 8-9, 4-5, 6-7	0 to 5 Volts
2-3, 8-9, 6-7	0 to 10 Volts
1-2, 9-10, 4-5, 6-7	± 2.5 Volts
1-2, 9-10, 6-7	± 5 Volts
1-2, 9-10, 5-6	± 10 Volts

Note: By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper J32 has three pins spaced at 0.100". J32 is located in the upper right section of the DAP, directly below J8.

The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If J32 is installed on pins 1-2 (pin 1 is on the left), all digital outputs will be reset to 0 at power-on. If J32 is installed on pins 2-3, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with J32 installed on pins 1-2. The voltage of the analog outputs at reset may vary by up to 5 millivolts when J32 is moved.

Input/Output Synchronization Header

The input/output synchronization header J22 has two pins spaced at 0.100". J22 is located approximately two inches above the left set of gold fingers on the Data Acquisition Processor. If a shunt is placed on J22, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector J13 has a single row of five pins on 0.100 inch centers. J13 is located at the upper left of the Data Acquisition Processor printed circuit board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock. See the Systems Manual for more information about using synchronous Data Acquisition Processors.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

5. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

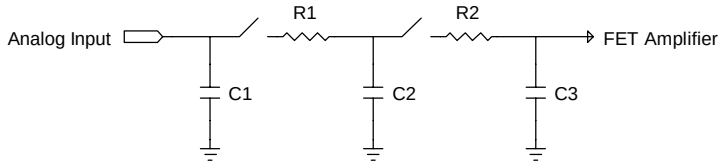
- The DC input impedance is very high.
- At high sampling rates, the signal source impedance should be low.
- Minimum sampling times are specified for unity gain.
- At gain 10, the fastest sampling rate is slower than the fastest sampling rate at gain 1.
- At gain 100 and 500, the fastest sampling rate is substantially slower than the fastest sampling rate at gain 1.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 2 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

Figure 2



The DAP 3200a has fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for fault-protected multiplexers.

Component	Value
R1	300Ω
R2	100Ω
C1	5 pF
C2	55 pF
C3	30 pF

Programmable Gain Amplifier

At gains other than unity, the programmable gain amplifier requires extra time to switch from pin to pin and then settle to full accuracy. The following table shows typical minimum sampling times for each Data Acquisition Processor at each gain.

Minimum Sample Times in µs at Gain:

	1	10	100	500
DAP 3200a	1.30	8	40	500

6. Clocks and Triggers

The Data Acquisition Processor is designed to operate using either internal clocks or external clocks. The Data Acquisition Processor has onboard crystal-controlled timers to provide an internal input sampling rate and output update rate, and also has provisions for external clocks for both input and output.

The Data Acquisition Processor has hardware control lines for an input clock, an output clock, an input trigger, and an output trigger. These lines all are TTL compatible. The input clock and the output clock both are positive-edge triggered.

The input and output clocks of the DAP 3200a have two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock.

The input trigger and output trigger on all models also have two modes, a one-shot mode and a level-triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications which require precise synchronization to external hardware or which are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. In applications with sampling rates of less than 10 KHz, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers, DAPL provides precise timing information. With hardware triggers, DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggers are implemented separately and may be used together.

External Input Clock

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Example:

```
IDEF A 5
   CLOCK EXTERNAL
   CLCLOCKING ON
   SET IPIPE0 S0
   SET IPIPE1 S1
   SET IPIPE2 S2
   SET IPIPE3 S3
   SET IPIPE4 S4
   TIME 1000
   . . . .
   END
```

External input clocking is enabled for the input procedure `A`. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of channel 0 (`S0`) to channel 4 (`S4`). The channels are converted in sequence with channel 0 synchronized to the positive edge of the external clock and each of the subsequent channels converted according to the `TIME` command. Channel 1 (`S1`) is converted 1000 µs following the edge of the external clock, channel 2 (`S2`) is converted 2000 µs following the edge of the external clock, up to channel 4 (`S4`) which is converted 4000 µs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of channels plus tSYNCH. The external clock may be as slow as required—there is no maximum period.

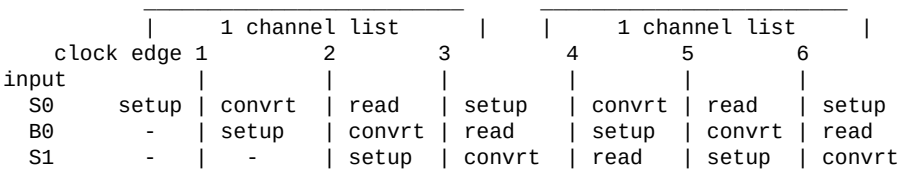
If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one channel. The channels are converted in sequence. Each channel is synchronized to a positive edge of the external clock. In the previous application, channel 0 (`S0`) is converted on the first edge of the external clock, channel 1 (`S1`) is converted on the second edge of the external clock, and so on up to channel 4 (`S4`), which is converted on the fifth edge of the external clock. The channel list then is repeated with channel 0 converted again on the sixth positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

Input Pipeline Timing

This section is of interest only when using external clocking or low latency with internal clocking.

The DAP 3200a has two pipeline stages for analog and digital inputs. The timing is the same for both inputs. An acquired value is read by the CPU after the following clock edge. This causes one sample period of time to be added to Data Acquisition Processor response latency. When channel list clocking is used with an external clock, the last value of the channel list is not read until the following external clock.

The following timing diagram illustrates the input timing for the DAP 3200a:



Note that `setup` indicates the setting-up of analog or digital input circuits before the value is sampled, `convrt` indicates when the value is held and converted to digital, and `read` indicates the value is read by the CPU. Each action occurs at or soon after the previous clock edge in the diagram.

The analog pipeline increases when analog and digital are used together to achieve aggregate input speeds higher than the maximum analog input rate. The digital input pipeline remains unchanged. The analog input pipeline increases to allow enough time for the analog-to-digital conversion.

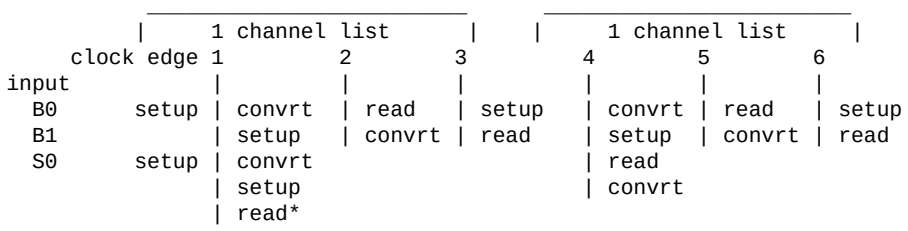
When arranging the channel list, the time between analog input samples must be equal to or greater than the minimum analog input sample time. Digital inputs can be placed between analog inputs to give the analog inputs enough time to convert. The number of clock cycles for analog conversion can be calculated by the following formula:

```
Cycles = roundup (Minimum Time/TIME)
```

`Minimum Time` is the minimum analog sample time for the Data Acquisition Processor model. This is 1.3 µs for the DAP 3200a. `TIME` is the sample time used in the input procedure.

An input configuration must start with `Cycles - 1` digital inputs before the first analog input. This guarantees that in any valid input configuration, there is only one clock period delay before DAPL can read each value. The first clock causes a garbage value to be read and ignored at the beginning of sampling; the last value in each burst is read in the first cycle of the subsequent burst. This, however, does not require an extra clock to read the expected number of values when external clocking is used because DAPL reads the very last value of a configuration without depending on external clocking.

The following timing diagram example shows how the analog input pipeline increases on a DAP 3000a/212 when analog and digital inputs are combined for an aggregate rate of 1.66 MHz. Note that for a `TIME` of 0.6, there are four clock cycles required for the analog input pipeline.



Note that the analog circuits set up for the next conversion while the current sample is being converted to digital. * indicates the value read is a garbage value. The value is thrown away by DAPL to ensure the correct order of values in input channel pipes.

It is important to note that if the first channel in an input configuration is a counter/timer input, there will be one more clock period delay added to the one extra clock period delay described above before DAPL can read each value. This additional delay is usually not desirable; therefore, it is strongly recommended that the first channel of an input configuration be of any type other than counter/timer if possible.

External Output Clock

For most applications, there is no need to provide an output clock source to the Data Acquisition Processor; the on-board timer provides a wide range of update frequencies with fine time resolution. The main use of an output clock is to precisely match the output update rate to a standard frequency.

The external output clock on the Data Acquisition Processor is a positive-edge triggered TTL signal. Similar to the external input clock, the output clock is activated by the command `CLOCK EXTERNAL` in an output procedure. The `TIME` command of an output procedure with output clocking enabled must be at least tSYNCH shorter than the external clock period. tSYNCH and other times are defined at the end of this chapter. Unlike the external input clock, the first external output clock pulse is recognized.

On the DAP 3200a, external output clocking has two modes. The first mode, called Channel List Clocking, starts output of an entire channel list on the positive edge of the external clock. The second mode outputs a single channel on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an output procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the input procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Hardware Output Trigger

There are two modes for the output trigger of Data Acquisition Processors. The first mode is a one-shot mode and the second mode is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an output procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an output procedure is started. Output updating does not start until the trigger line is high. Updating continues until a `STOP` command is issued or the number of updates specified by the `COUNT` command of the output procedure is reached. The first updated value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the output procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external output trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, output updating may start and stop repeatedly, depending on the level of the trigger signal. The output is updated continuously when the trigger signal is high. Output updating stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When output clocking is configured in Channel List Clocking mode, the output is stopped only at channel list boundaries. When output clocking is configured to clock single channels, the output may stop after any channel. The effect of this is that the start of output is precisely synchronized to the positive edge of the trigger signal, assuming that output has stopped. Output stops when the Data Acquisition Processor has completed output of either a channel list or a channel. When output has been stopped with the gated trigger, synchronization of output to the positive edge of the trigger signal is the same as for the one-shot mode.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `FIRFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling or output updating starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling or output updating may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

The Data Acquisition Processor acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Using the Output Trigger with External Output Clocking

Output triggering may be used with external output clocking. To guarantee recognition of an external clock, the external trigger must occur at least tTCSETUP before the positive edge of the external clock.

Timing tables

tSYNCH	200 ns	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input and output trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tITRIG_MAX	250 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held
tOUTSKEW	30 ns	Time from output clock until start of DAC slewing

7. Recalibration

Each Data Acquisition Processor is burned in and then calibrated by Microstar Laboratories. The accuracy of this calibration is sufficient for most applications. Accuracy is affected by three factors:

- the operating temperature of the Data Acquisition Processor
- drift in the Data Acquisition Processor circuitry
- analog voltage range selection.

The operating temperature is determined by a number of factors. If the Data Acquisition Processor is operated inside a personal computer, the operating temperature is affected by the number of expansion boards, power supply loading, fan efficiency, etc.

Component drift depends on total operating time of the unit as well as the number of times the unit has been powered up and down.

Changes to analog voltage ranges generally require that the Data Acquisition Processor be recalibrated.

For applications requiring high accuracy, occasional recalibration may be necessary. For high absolute accuracy, the Microstar Laboratories calibration sequence requires that measurements be made using a 4.5 digit digital voltmeter with a DC accuracy of .024% (244 ppm) or better. In most applications, only relative accuracy is important, so recalibration with a less accurate digital voltmeter may be acceptable. Calibration also requires a variable voltage source with high stability.

Because calibration requires significant setup time, it generally is best to send Data Acquisition Processors to Microstar Laboratories for recalibration. Calibration is available from Microstar Laboratories for a nominal fee.

CALDAP

CALDAP is a program which uses a PC to recalibrate Data Acquisition Processor analog input circuitry. Recalibration may be necessary if analog voltage range jumpers are changed, or if the Data Acquisition Processor factory calibration has drifted.

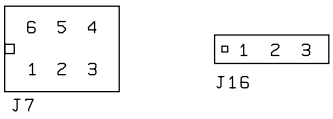
Equipment Requirements

Data Acquisition Processor calibration requires the following equipment:

- A 4 1/2 digit digital voltmeter (DVM).
- A -10 volt to +10 volt adjustable voltage source. The voltage source must be very stable and must have an output impedance of less than 500 ohms.

Connector Numbering

CALDAP prompts refer to particular pins of Data Acquisition Processor connectors. A diagram with connector locations is located at the beginning of Chapter 4. Pin 1 of a connector with a single row of pins is identified by a dot, and pin 1 of a connector with two rows of pins is identified by a notch—pins are numbered in a counter-clockwise direction in the same manner as an integrated circuit, as in the following examples:



A PC-bus extender card can be used to permit easier access to the connectors on the Data Acquisition Processor.

Preparing the Data Acquisition Processor

The Data Acquisition Processor must have power applied for at least two hours before calibration.

For a DAP 3200a, configure the Data Acquisition Processor hardware as follows:

1. Connect the `S1` pin to the `G1` pin.
2. Apply the adjustable voltage source across `S0` and `G0`.
3. Connect the DVM to sense `S0` relative to `G0`.
4. Connect the `S15` pin to the `S14` pin. Also connect these two pins to `DAC1 OUT`.

Starting CALDAP

CALDAP is included on the Data Acquisition Processor diskettes in the subdirectory `\DAP\CALDAP`. The active drive and the active directory should be set so that the CALDAP program is in the current directory. For example:

```
C:
CD \DAP\CALDAP
```

CALDAP should be started by typing CALDAP at the DOS prompt. CALDAP accepts five optional switches:

```
CALDAP [/CF:DAP3201E\aaaa] [/Rxyz] [/FORCECAL] [/Scccc] [/M]
```

The parameter `aaaa` selects the type of calibration. The calibration types are:

`RANGE`	0 to 5V, ± 5V and ± 10V input range amplifier calibration..
`PGA`	PGA gain calibration.
`DACS`	DAC calibration.
`CAL`	Complete calibration procedure.

The entire calibration sequence is required when the input voltage range is changed, unless it is changed to or from ±2.5V. The PGA gain calibration trims the 10, 100, and 500 gains of the programmable gain amplifier. The DAC calibration calibrates the offsets and gains of the digital-to-analog converters. The complete calibration performs each of the above operations, as well as calibration of the instrumentation amplifier. Microstar Laboratories recommends that a complete calibration *not* be performed unless specifically required. Calibration is available from Microstar Laboratories for a nominal fee.

The second CALDAP parameter determines calibration voltage ranges. The parameters `x`, `y`, and `z` are numbers selecting voltage ranges. The `x` parameter selects the analog input voltage range:

0 -2.5 to +2.5 volts
2 -5 to +5 volts
3 -10 to +10 volts
5 0 to +5 volts

The `y` and `z` parameters select the analog output voltage ranges of `DAC0` and `DAC1`, respectively:

0 -2.5 to +2.5 volts
2 -5 to +5 volts
3 -10 to +10 volts
5 0 to +5 volts
6 0 to +10 volts

For example, the following CALDAP command performs complete Data Acquisition Processor calibration with a -10 to +10 volt analog input range and a -10 to +10 volt analog output range on both DACs:

```
CALDAP /CF:DAP3201E\CAL /R333
```

If no range parameter is specified on the CALDAP command line, `/R222` is assumed.

The `/FORCECAL` parameter causes calibration to start immediately upon entry into CALDAP.

The `/Scccc` parameter is for custom Data Acquisition Processors. This parameter should not be specified on the CALDAP command line for normal Data Acquisition Processors. Contact Microstar Laboratories for information on calibrating Data Acquisition Processors with custom analog input sections.

The `/M` parameter is used internally by Microstar Laboratories and should not be specified on the CALDAP command line.

Calibrating the Data Acquisition Processor

Once the PC is executing CALDAP, a `<Ctrl-E>` command from the keyboard is used to begin calibration. This is not necessary if the `/FORCECAL` parameter is used, in which case calibration begins automatically.

CALDAP performs a series of calibration steps. Each calibration step has a unique step number. There are several different types of calibration steps:

1. Configuration step. This step sends configuration information to the Data Acquisition Processor. No user interaction is required.
2. Prompt step. This step waits for you to perform a specific action. The action may be changing a jumper or may be changing the voltage of the variable voltage source. When CALDAP prompts to change the variable voltage, the jumper pin numbers to use for the signal and the ground sense of a DVM are provided within parentheses. For example, a prompt of `Inst Out (J7:3, J7:1)` specifies that `J7:3` is the signal connection for the DVM and `J7:1` is the ground sense connection for the DVM.
3. Potentiometer adjustment step. This step allows interactive adjustment of a potentiometer. CALDAP displays the letter of a particular potentiometer and a sequence of arrows which indicate the direction in which to turn the potentiometer. Turn the potentiometer until the arrow display is centered and the arrows are replaced by a vertical line.

During calibration, the following keys perform control functions:

`<enter>`	goes to next step
`<backspace>`	goes to previous step
`<esc>`	aborts calibration

After aborting or finishing calibration, a `<Ctrl-Z>` command from the keyboard will end the CALDAP program. Optionally, the user may enter a `<Ctrl-E>` command from the keyboard to restart calibration. Several calibration sequences are iterative—a series of calibration steps is repeated until potentiometer adjustments are sufficiently accurate. In most cases, no iteration is required during recalibration; if a particular potentiometer is adjusted more than three times, CALDAP probably has detected instability in the calibration sequence. This usually is caused by excessive noise in the adjustable external voltage supply, or possibly by damaged analog circuitry on the Data Acquisition Processor.

Appendix A: Declaration of Conformity

Declaration of Conformity

Microstar Laboratories
2265 116th Avenue NE
Bellevue, WA 98004

Microstar Laboratories declares that the DAP 3200a conforms to the following Directive and Standards:

Electromagnetic Compatibility (EMC):

EMC Directive 89/336/EEC

EN 55022	Emission Standard
EN 50082-1	Immunity Standard

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