DAP 4400a Manual

Installation Guide and
Connector Reference

Version 1.00

Microstar Laboratories, Inc.

Microstar Laboratories, Inc.
2265 116 Avenue N.E.
Bellevue, WA 98004
Tel: (425) 453-2345
Fax: (425) 453-3199
http:// www.mstarlabs.com

Part Number MSHM008-01

Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 4400a is a high-performance Data Acquisition Processor specialized for fast analog sampling.

Features:

- i486DX4 CPU
- PCI bus interface
- 16 Megabytes DRAM
- 50 ns TIME resolution
- 800K samples per second per channel
- 3.2 million samples per second aggregate
- inherent simultaneous sampling of 4 input pins
- no output and no digital port
- ±2.5 volt, ±5 volt, and ±10 volt ranges

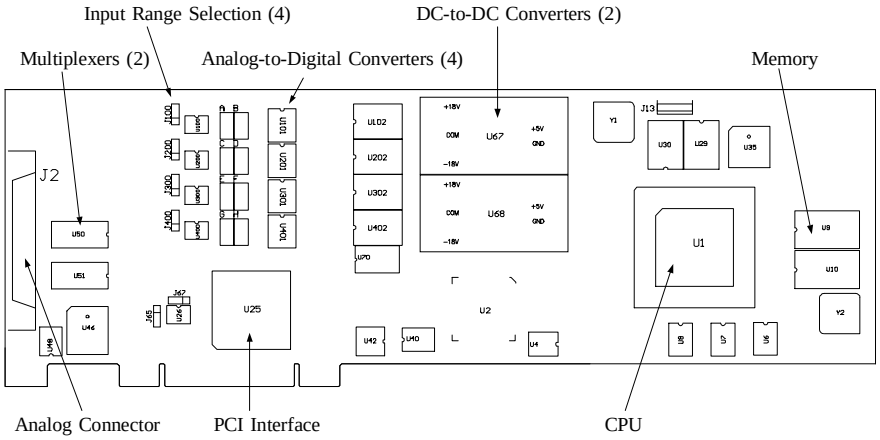


Figure 1. DAP 4400a Components

Overview of the DAP 4400a

The DAP 4400a uses four analog-to-digital converters. Each analog-to-digital converter is connected to four single-ended input pins. When the input pins are sampled, sampling occurs in groups of four, with one input on each multiplexer sampled simultaneously with one pin on each of the other analog-to-digital converters. Each analog-to-digital converter is capable of converting 800K samples per second, making a maximum aggregate sample rate of 3.2 million samples per second.

The onboard operating system for the DAP 4400a is DAPL 2000, which is optimized for 32 bit operation. DAPL 2000 has been further customized for the DAP 4400a. A few commands, like the `SET` command, have changed for the DAP 4400a because of the specialized input configuration.

About this Manual

This manual includes hardware and software installation instructions, a hardware connector reference, application examples, analog expansion pin mapping, and updated information for support software. Two other manuals accompany this manual:

- The DAPL Manual contains a complete DAPL 2000 reference. Please refer to the "DAPL commands" chapter of the manual for information about command changes with the DAP 4400a.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications. Please note that some commands have a new syntax for the DAP 4400a, and note that analog output and digital input and output is not available on the DAP 4400a.

2. Installation, Testing, & Troubleshooting

Installing a Data Acquisition Processor involves the following steps:

1. Install the Data Acquisition Processor.
2. Install the DAP Software.
3. Test the Installation.

Installation instructions are provided in this chapter. If there are any problems with installation, please read the troubleshooting guide at the end of this chapter.

Data Acquisition Processor Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge because it contains many high-speed analog and digital components. To protect the Data Acquisition Processor, observe the following precautions:

- Wear a grounding strap when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC offers limited protection.
- If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

System Requirements

The DAP 4400a is compatible with 5V 32 bit PCI Bus slots that support bus-mastering in 486/Pentium/Pentium Pro/Pentium II computers and requires Windows 95, Windows 98 or Windows NT 3.51 or later.

Cooling Space Requirement

The DAP 4400a uses a clock-tripled processor that requires a heat sink for cooling. Ideally, there should be enough empty space around the heat sink to allow adequate cooling. The DAP 4400a uses a short heat sink that allows a full-length expansion card to be installed in the adjacent slot. If a full-length expansion card is installed in the adjacent slot near the heat sink, the user must make sure there is an air flow of at least 400 linear feet per minute over the heat sink to guarantee adequate cooling.

Caution: Insufficient air flow can damage the Data Acquisition Processor.

Installing the Data Acquisition Processor

Caution: Do not install the Data Acquisition Processor while the PC is on.

To Install the Data Acquisition Processor:

1. Turn off the PC and remove the PC's cover.
2. Insert the Data Acquisition Processor into any free PCI slot.
3. Screw down the back panel of the Data Acquisition Processor to the back chassis of the PC.

The Data Acquisition Processor requires approximately 15 Watts from the PC's power supply. If your system behaves erratically with the Data Acquisition Processor installed, the PC may need a larger power supply.

Installing Several Data Acquisition Processors

Many Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. The driver supports up to 14 Data Acquisition Processor boards in one PC. However, the number of Data Acquisition Processor boards is limited by the number of available PCI slots in the PC. Each Data Acquisition Processor requires one PCI slot.

Installing DAP Software

Before installing the DAP Software, make backup copies of the diskette(s). Put the originals in a safe place, and use the backup disks for installation.

Installation Under Windows NT

In Windows NT 3.51 or 4.0, run the `SETUP.EXE` program that comes with the release diskette and follow the on-screen instructions.

Installation Under Windows 95 or Windows 98

Windows 95 and Windows 98 support plug-and-play hardware device installation. For first time installation, use the operating system's "Found (Add) New Hardware Wizard." When the Data Acquisition Processor is plugged into a PCI slot for the first time, the Wizard will begin and prompt you to install the device drivers. Insert the release diskette into floppy drive `a:` and follow the Wizard instructions, specifying "`a:\`" or selecting the floppy drive as the source drive. Click "OK" or "Next" (depending on the version of Windows) until the last Wizard dialog box appears. Click "Finish" to complete this part of the installation. At this point, `SETUP.EXE` will automatically continue with the rest of the installation.

For subsequent installations under Windows 95 or Windows 98, just run `SETUP.EXE` from the release diskette.

Testing Installation

To test the software installation, run the `DAPlog.EXE` program.

Troubleshooting

If the Accel32 Service will not start, check the host PC hardware manual to make sure that the particular PCI slot that the DAP uses supports bus-mastering. If necessary, switch to a different slot.

3. DAP 4400a Connectors

This chapter discusses the interface connectors on the DAP 4400a series. Diagrams and documentation for the analog input connector, synchronization connector, and analog input range selection jumpers are provided in this chapter.

Figure 2 shows component placement outlines of the DAP 4400a. The only components shown are connectors, whose labels begin with the letter `J`, some integrated circuits, whose labels begin with the letter `U`, and trim potentiometers, whose labels are single letters.

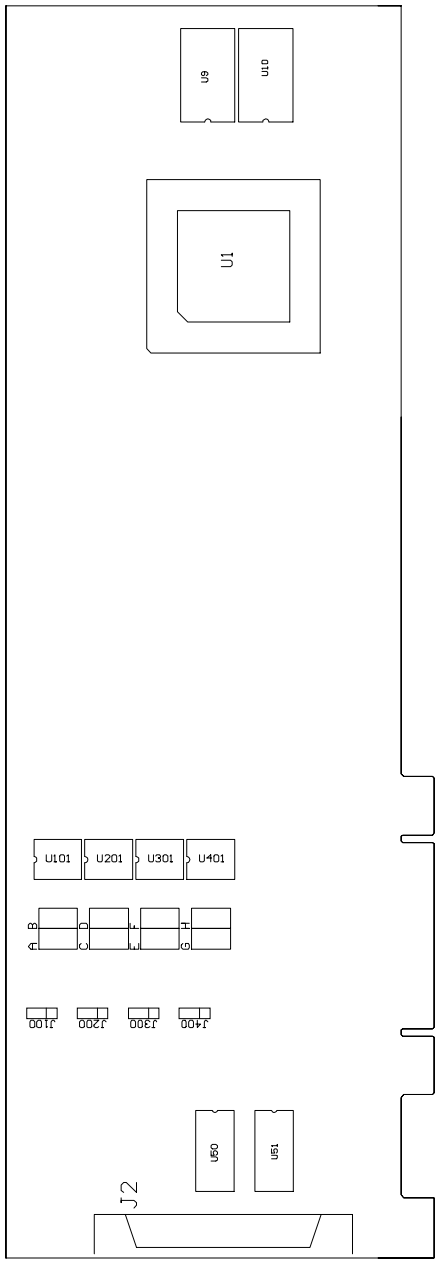
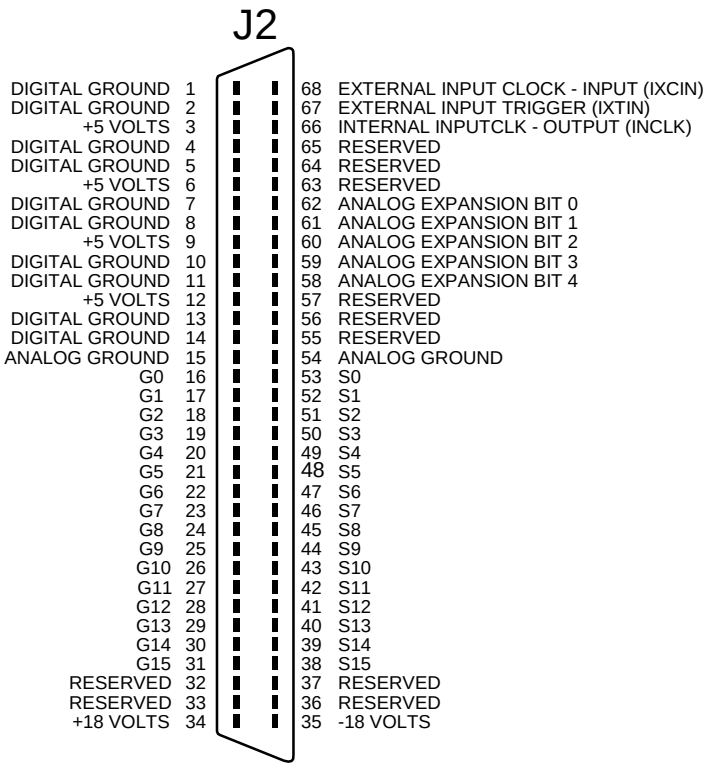


Figure 2. DAP 4400a

Analog Input Connector

Analog voltages are connected to the Data Acquisition Processor through a 68 pin analog connector on the back panel of the PC. This connector is located on the left side of the Data Acquisition Processor and is labeled J2. It has a double row of pins on 0.050 inch centers. The connector is 3M part number 10268 52E2VC or AMP part number 2 178238 8. It mates with discrete wire connector 3M part number 10168-6000EC or AMP part number 2 175677 8. Both connectors are shielded and are compatible with round cable. The analog input connector also mates with insulation displacement ribbon cable connector 3M part number 10168 8100EE. The insulation displacement connector is compatible with 0.025" pitch ribbon cable.

Looking at the analog connector from the back of a PC, the pin numbering is:



NOTE: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Inputs are indicated by `S0` through `S15`; their corresponding ground inputs are `G0` through `G15`.

A single-ended analog signal should be connected to an analog input pin with the signal ground connected to the corresponding ground pin, for example to pins 16 and 53.

Termination boards to connect all lines of the analog connector to discrete wires are available from Microstar Laboratories.

The DAP 4400a features fault-protected input multiplexers. Fault protected input multiplexers allow signals to be connected to the Data Acquisition Processor with power off and allow a higher input voltage without damaging the inputs. Spare fault-protected input multiplexers are available from Microstar Laboratories.

Analog input signals should be within the range from -25 volts to +25 volts, relative to the ground of the Data Acquisition Processor. Input signals may be applied to the Data Acquisition Processor when the PC's power is off.

The analog connector of the Data Acquisition Processor includes pins for analog power supply voltages. Pin 15 is analog power ground. Pins 34 and 35 are connected to +18 volt and -18 volt analog supplies, respectively. The maximum allowable current drain from these supplies is 20 milliamps per side. These supplies can be used for low current, low noise devices such as external multiplexers. To supply power to other devices, either use an external supply or use the 5 volt digital power supply found on the analog control connector with an external DC-to-DC converter.

Pins 58 - 62 provide TTL-compatible analog input expansion control signals. These control signals are the five highest order address bits of the input pin group number (bits 2-6). The analog input expansion control signals are valid from immediately after one sample to immediately after the next sample. The analog input expansion control bits designate the address of the next sample to be taken.

External analog input expansion boards are available from Microstar Laboratories. Each input expansion board allows up to 64 single-ended inputs.

The analog connector has an input pin for an active high external input trigger. The external input trigger can be used to control when input sampling occurs. To use the external trigger, an `HTRIGGER` command is needed in the active input procedure. The external trigger is ignored if there is no `HTRIGGER` command in the active input procedure.

The external input trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a 10k Ohm pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected. Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off.

The analog connector has an input pin for an external input clock. The input pin should be used to connect an external input clock. The analog connector also has an output pin for the input clock. The output pin is the buffered output of the internal clock circuit.

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100” centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has one hardware configuration option which determines the analog input voltage range.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. buffer amplifier
3. range amplifier
4. analog-to-digital converter with sample and hold amplifier

Analog signals pass through all of these functional units. Jumpers determine the analog input voltage range for each of the four analog input sections. Each section may be configured independently. The Data Acquisition Processor should be recalibrated after changing the input voltage range.

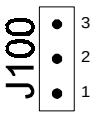
A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The DAP 4400a has only bipolar input ranges.

A signal is single ended if it is measured relative to ground. A signal is differential if it is measured relative to another signal The DAP 4400a accepts only single-ended inputs; there are no provisions for differential inputs.

Analog Input Voltage Range Configuration

The following connectors control the analog input voltage range of the DAP 4400a. Note that changing voltage ranges generally requires recalibration.

Connectors `J100`, `J200`, `J300`, and `J400` select the input signal range of the range amplifier. `J100` selects the range for channels 0 through 3, `J200` selects the range for channels 4 through 7, `J300` selects the range for channels 8 through 11, and `J400` selects the range for channels 12 through 15.



One jumper should be placed on each of `J100`, `J200`, `J300`, and `J400` as follows:

Jumper	Input signal range
1-2	± 2.5 volts
None	± 5 volts
2-3	± 10 volts

NOTE: Regardless of the input voltage range, positive and negative signals may range from -25 volts to +25 volts without damaging the Data Acquisition Processor.

The following table summarizes the DAP 4400a jumper connections:

ADC Range	J100, inputs 0-3	J200, inputs 4-7	J300, inputs 8-11	J400, inputs 12-15
± 2.5v	1 - 2	1 - 2	1 - 2	1 - 2
± 5v*	None*	None*	None*	None*
± 10v	2 - 3	2 - 3	2 - 3	2 - 3

* Factory Configuration

Synchronization Connector

The synchronization connector `J13` has a single row of five pins on 0.100 inch centers. `J13` is located along the top edge of the Data Acquisition Processor near the right side of the board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

4. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

- The DC input impedance is very high.
- At high sampling rates, the signal source impedance should be low.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 3 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

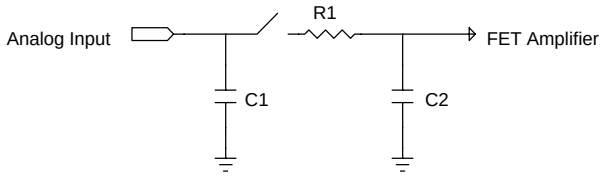


Figure 3

The DAP 4400a features fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for the DAP 4400a.

Component	Resistance/Capacitance
R1	300Ω
C1	5 pF
C2	30 pF

5. Clocks and Triggers

The Data Acquisition Processor is designed to operate either using internal clocks or external clocks. The Data Acquisition Processor has onboard crystal controlled timers to provide an internal input sampling rate and also has provisions for external clocks.

The DAP 4400a has hardware control lines for an input clock and an input trigger. These lines are TTL compatible. The input clock is positive edge triggered.

The input clock has two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single pin group on the positive edge of the clock.

The input trigger also has two modes, a one-shot mode and a level triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism suitable for most applications. For those applications that require precise synchronization to external hardware or that are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. In applications with low enough sampling rates, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers DAPL provides precise timing information. With hardware triggers DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggering are implemented separately and may be used together.

External Input Clock

For most applications, there is no need to provide an input clock source to the Data Acquisition Processor; the on-board timer provides a wide range of sampling frequencies with fine time resolution. The main use of an external input clock is to precisely match the sampling rate to a standard frequency.

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least `tSYNCH` less than the period of the external clock. `tSYNCH` is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel group list on the positive edge of the external clock. The second mode converts a single pin group on the positive edge of the external clock. The selection between the modes is made by a parameter to the `CLCLOCKING` command in an input procedure. The two options for `CLCLOCKING` are `ON` and `OFF`. The default is `ON`.

Example:

```
  IDEF A 4
CLOCK EXTERNAL
CLCLOCKING ON
SET(0..3) SPG0
SET(4..7) SPG1
SET(8..11) SPG2
SET(12..15) SPG3
TIME 1000
. . . .
END
```

In this application, external input clocking is enabled for the input procedure A. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of pin group 0 (`SPG0`) to pin group 3 (`SPG3`). The pin groups are converted in sequence with pin group `SPG0` synchronized to the positive edge of the external clock and each of the subsequent pin groups converted according to the TIME command. Pin group 1 (`SPG1`) is converted 1000 µs following the edge of the external clock, pin group 2 (`SPG2`) is converted 2000 µs following the edge of the external clock, and pin group 3 (`SPG3`) is converted 3000 µs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of pin groups plus `tSYNCH`. The external clock may be as slow as required—there is no maximum period.

If single group clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one pin group. The pin groups are converted in sequence. Each pin group is synchronized to a positive edge of the external clock. In the previous application, pin group 0 (`SPG0`) is converted on the first edge of the external clock, pin group 1 (`SPG1`) is converted on the second edge of the external clock, and so on up to pin group 3 (`SPG3`), which is converted on the fourth edge of the external clock. The pin group list then is repeated with pin group 0 converted again on the fifth positive edge of the external clock. When using single group clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus `tSYNCH`. The external clock may be as slow as required—there is no maximum period.

Input Pipeline

The DAP 4400a has one pipeline stage for analog and digital inputs. The timing is the same for both inputs. An input is acquired and read by the CPU on the same input clock cycle. Note that this is an improvement over the DAP 3200a pipeline, where an input is acquired on one input clock cycle, and that acquired value is read by the CPU on the next input clock cycle.

The DAP 3200a and other ISA models of Data Acquisition Processors generate an additional input clock cycle when input sampling is stopped, in order for the CPU to read the last acquired value. When synchronizing multiple Data Acquisition Processors, the master generates the additional input clock cycle. The slave units depend on this additional clock cycle to read the last acquired value.

Because of its improved input pipeline, the DAP 4400a does not generate an additional input clock when input sampling is stopped. Therefore, the DAP 4400a must be configured as a slave unit when synchronizing the DAP 4400a with ISA models of Data Acquisition Processors.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued, or the number of samples specified by the `COUNT` command of the input procedure is reached, or all onboard memory is consumed. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ± `tSYNCH` of the `TIME` command of the input procedure. `tSYNCH` is defined at the end of this chapter. The active period of the external input trigger must be greater than 60ns to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single pin groups, the input is stopped on pin group boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a pin group. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may be determined only if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT32`, and `FIRFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling starts on a single event, so all timing information is relative to the trigger event. In the case of a gated trigger, sampling may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

The Data Acquisition Processor acts upon the first external clock cycle after the trigger has been asserted, assuming input sampling has stopped. To guarantee recognition of an external trigger, the external trigger must occur at least 50 ns before the positive edge of the external clock.

Timing tables

tSYNCH	200 ns	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tITRIG_MAX	200 ns (DAP 4400a only)	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held

6. Sample Applications

The Applications Manual contains many sample applications for use with Data Acquisition Processors. However, the DAP 4400a uses a different input configuration, which requires a new syntax for a few DAPL commands.

The most significant change to the DAPL syntax for the DAP 4400a is how inputs are configured. Also, be aware that since the DAP 4400a samples in groups of four, data may need to be sent to the host PC differently. For example, if you are concerned with the inputs of only two channels, you do not need to send all four sampled channels to the PC.

In this chapter, two applications from the Applications Manual have been rewritten for the DAP 4400a. Following the syntax changes that were made in these examples, many examples in the Applications Manual can be modified for use with the DAP 4400a. Please note that analog output applications and digital input and output applications will not work with the DAP 4400a.

Example 1—Sampling Inputs Sequentially

This application configures the DAP 4400a to sample three input signals sequentially and send the digitized values to the PC. Since the DAP 4400a always samples input pins in groups, this application is different than for other Data Acquisition Processors where certain input pins must be sampled (one from each group).

This application is similar to Application 1 in the Applications Manual. The `IDEFINE`, `SET`, and `COPY` commands have been changed for the DAP 4400a. The same single-ended input pins are used, but the differential input has been changed to single-ended input `S8`.

The following DAPL commands configure the Data Acquisition Processor for this application. Indentation is optional since DAPL ignores extra spaces.

```
RESET
  IDEFINE A 3
  SET IPIPES(0..3)  SPG2 ;SPG2 includes S2 connected to IP0
  SET IPIPES(4..7)  SPG1 ;SPG1 includes S5 connected to IP5
  SET IPIPES(8..11) SPG0 ;SPG0 includes S8 connected to IP10
  TIME 100               ;100 us between each group
  END
PDEF B
  COPY(IPIPES(0,5,10),$BINOUT)
  END
```

The `RESET` command on the first line clears all definitions and errors. It is a good idea to start each application with a `RESET`.

The next line begins an input procedure definition. An input procedure definition starts with the word `IDEFINE` and ends with the word `END`. `IDEFINE` usually is abbreviated to `IDEF`. The `IDEFINE` command requires the name of the input procedure and the number of input channel groups read by the input procedure. "`A`" is the name chosen for the input procedure in this application.

The line `IDEFINE A 3` configures the Data Acquisition Processor to sample three input channel groups, or 12 single-ended input pins. The `SET` commands associate input channel groups with pin groups. Since inputs are connected to `S2`, `S5`, and `S8`, pin groups `SPG2`, `SPG1`, and `SPG0` must be used. The three `SET` commands used connect input channel 0 (`IP0`) to single-ended input `S2`, `IP5` to single-ended input `S5`, and `IP10` to single-ended input `S8`.

The `TIME` command sets the sampling time to 100 microseconds. Since the input configuration samples three pin groups, each group is sampled every 300 microseconds.

`END` marks the end of the input procedure definition.

The word `PDEFINE` begins a processing procedure definition. `PDEFINE` is usually abbreviated to `PDEF`. The `PDEFINE` command is followed by the name of the processing procedure, which is `B` in this application. You are free to choose other names for procedures in your applications.

The COPY command transfers binary data from input channels 0, 5, and 10 to the binary communications pipe $BINOUT. The Data Acquisition Processor transfers binary data in $BINOUT directly to the PC. The COPY task continues until sampling is stopped.

END marks the end of the processing procedure definition.

Data collection begins when a START command is issued:

```
START A, B
```

The COPY task transfers data values from each input channel pipe in order. The host program running on the PC must know the number of data channels sent from the Data Acquisition Processor in order to correctly display the data. Some programs automatically determine the number of data channels by examining the DAPL command file.

To stop sampling, issue a STOP command. This command stops the input procedure and the processing procedure. Analog sampling is stopped and the COPY task is halted. The application can be restarted by reissuing the START command.

This application can be simplified if the inputs are sampled simultaneously. To do this, all inputs must be from one pin group. In the following example pin group SPG0 is used, which contains pins S0, S4, and, S8, and S12. Samples from S0, S4, and S8 are sent to the PC with the COPY command:

```
RESET
  IDEF A 1
  SET(0..3)  SPG0
  TIME 300
  END
PDEF B
 COPY(IPIPES(0..2),$BINOUT)
 END
```

Note that TIME was adjusted to make the data rate the same as with the first example.

Example 2—True Simultaneous Sampling

Some applications require sampling two or more analog inputs simultaneously. The DAP 4400a can sample up to four channels simultaneously. In this application, the DAP 4400a samples single-ended inputs `S1`, `S5`, `S9`, and `S13` simultaneously, with all four channels being sampled every 1000 microseconds.

This application is similar to Application 33 from the Applications Manual.

```
RESET
IDEF A 1
  SET IPIPES(0..3),SPG1
  TIME 1000
END
```

The term `IPIPES` is optional for the `SET` command.

All four channels defined in the `SET` command will be sampled. Extra channels can be ignored if you need the data from only two or three channels.

Example 3—Simulated Simultaneous Sampling

This application uses `FIRFILTER` commands to perform a time-shifting interpolation on 16 channels of raw data.

The DAP 4400a samples data in groups of four channels. If all 16 analog inputs are sampled, the normal sampling sequence is to sample four channels, then, one interval later, sample the next four channels, and so on.

Sometimes it is necessary to get a "snapshot" of data, or to look at what is happening to all input data channels at one instant. This is known as simultaneous sampling. The DAP 4400a hardware is designed for simultaneous sampling of up to four input channels. If more than four channels are involved, a software correction to simulate simultaneous sampling is possible using the DSP features of the DAP 4400a hardware and software. In effect, the correction algorithms construct local approximating curves for each data sequence, and use the approximating curves to estimate the sample values that would have been recorded if all of the signals had been sampled at the same time. (Technically speaking, the approximating curves used in this application are the least-squares best fit of a cubic polynomial model.)

The approximation process has some drawbacks for the case of very high frequency signals because the approximation tends to suppress very rapid local changes in the data. However, if the rapid local changes are due to high frequency noise, the noise-suppression side effect is beneficial.

To create a software simulation of simultaneous sampling for sixteen channels, samples of all four channels groups need to be taken in a repeating sequence.

The first four channels do not need to be corrected, but this application applies filtering so that all 16 channels experience the same high-frequency noise reduction. The interpolation approximates the data in last twelve channels for the time at which the first channel group was sampled by “time-shifting” the data in the second, third and fourth channel groups by 1, 2 and 3 sampling intervals, respectively.

The following DAPL commands configure the DAP 4400a for this application:

```
RESET
VECTOR SHIFT000 = (-3121, 4681, 9362, 10923, 9362, 4681,
  -3121)
VECTOR SHIFT025 = (-3700, 6845, 11160, 10825, 7418, 2517,
  -2298)
VECTOR SHIFT050 = (-3950, 8923, 12727, 10533, 5413, 439,
  -1317)
VECTOR SHIFT075 = (-3785, 10831, 13977, 10045, 3431, -1469,
  -262)
PIPES  P0, P1, P2, P3, P4, P5, P6, P7, P8, P9,
PIPES  P10, P11, P12, P13, P14, P15
IDEF  SAMP 4
  SET IP(0..3)   SPG0
  SET IP(4..7)   SPG1
  SET IP(8..11)  SPG2
  SET IP(12..15) SPG3
  TIME  20.00
  END
PDEF  FILT
  FIRFILTER( IP0,  SHIFT000, 7, 1, 0, 0, P0 )
  FIRFILTER( IP1,  SHIFT000, 7, 1, 0, 0, P1 )
  FIRFILTER( IP2,  SHIFT000, 7, 1, 0, 0, P2 )
  FIRFILTER( IP3,  SHIFT000, 7, 1, 0, 0, P3 )
  FIRFILTER( IP4,  SHIFT025, 7, 1, 0, 0, P4 )
  FIRFILTER( IP5,  SHIFT025, 7, 1, 0, 0, P5 )
  FIRFILTER( IP6,  SHIFT025, 7, 1, 0, 0, P6 )
  FIRFILTER( IP7,  SHIFT025, 7, 1, 0, 0, P7 )
  FIRFILTER( IP8,  SHIFT050, 7, 1, 0, 0, P8 )
  FIRFILTER( IP9,  SHIFT050, 7, 1, 0, 0, P9 )
  FIRFILTER( IP10, SHIFT050, 7, 1, 0, 0, P10 )
  FIRFILTER( IP11, SHIFT050, 7, 1, 0, 0, P11 )
  FIRFILTER( IP12, SHIFT075, 7, 1, 0, 0, P12 )
  FIRFILTER( IP13, SHIFT075, 7, 1, 0, 0, P13 )
  FIRFILTER( IP14, SHIFT075, 7, 1, 0, 0, P14 )
  FIRFILTER( IP15, SHIFT075, 7, 1, 0, 0, P15 )
  MERGE( P0,P1,P2,P3,P4,P5,P6,P7,P8,P9,P10,\
         P11,P12,P13,P14,P15,$BINOUT )
  END
START SAMP,FILT
```

The `RESET` command on the first line clears all definitions and errors.

The four VECTOR commands define data for four filters. SHIFT000 is the filter data used for the first channel group, SHIFT025 is the filter data used for the second channel group, SHIFT050 is the filter data used for the third channel group, and SHIFT075 is the filter data used for the fourth channel group.

The PIPES commands define 16 data pipes for use by the FIRFILTER commands.

The input procedure SAMP configures input channel pipes 0-15 with the four input pin groups SPG0-SPG3. This associates each analog input pin with one input channel pipe.

The TIME command sets the sampling interval to 20 microseconds. Since data is being time-corrected for four channel groups, the results will be an approximation for simultaneous sampling every 80 microseconds.

The processing procedure FILT is where the interpolation of data is configured. Each FIRFILTER command receives data from one input channel. Depending on which group the channel was sampled in, one of the four filter vectors is applied to the data. After the data is filtered, each is sent to a data pipe.

The MERGE command sends all filtered data to the PC through the binary communications pipe $BINOUT.

END marks the end of the processing procedure.

START begins processing of the input procedure SAMP and the processing procedure FILT. Sampling can be stopped by issuing a STOP command.

7. Appendix A: Analog Expansion Pin Mapping

Expansion board MSXB 018 has four connectors for expansion. Each connector has 16 inputs numbered `S0` to `S15`, for a total of 64 analog inputs per board. The DAP 4400a can use up to eight analog input expansion boards, for a total of 512 analog inputs, or 128 pin groups. This Appendix documents how the expansion board pin numbers map to pin group numbers used in the DAPL `SET` commands.

For the DAP 4400a, all channel groups in an input procedure must be explicitly configured.

Microstar Laboratories strongly suggests that if you are using analog expansion, use `OPTION AINEXPAND=ON`. This option maps the pins of the Analog Input Expansion Board to match the order on the Data Acquisition Processor analog connector.

With `AINEXPAND ON`, the mapping for one expansion board will be:

Pin Group	Analog Expansion Pin Numbers
SPG0	S0 on each termination board
SPG1	S1 on each termination board
SPG2	S2 on each termination board
SPG3	S3 on each termination board
SPG4	S4 on each termination board
SPG5	S5 on each termination board
SPG6	S6 on each termination board
SPG7	S7 on each termination board
SPG8	S8 on each termination board
SPG9	S9 on each termination board
SPG10	S10 on each termination board
SPG11	S11 on each termination board
SPG12	S12 on each termination board
SPG13	S13 on each termination board
SPG14	S14 on each termination board
SPG15	S15 on each termination board

For a second expansion board, SPG16 maps to S0 on each termination board SPG17 maps to S1, etc. Because of the sequential numbering of pin groups, it is important to keep track of expansion board and termination board sequencing.

Within a channel group, the four channels are connected to the four corresponding pins on connectors J5, J4, J3 and J2 in that order. For example, if the channel group IPIPES(0..3) is connected to the expanded SPG0, then IP0 is connected to S0 on connector J5 of the expansion board, IP1 to S0 on connector J4, IP2 to S0 on connector J3, and IP3 to S0 on connector J2. The following table shows how DAPL pin numbers map to analog expansion pins and termination board inputs.

DAP 4400a Expansion Pin Mapping

(OPTION AINEXPAND=ON)

DAPL Pin	Connector Number	Connector Pin	Termination Board Label
S0	J5	53	S0
S1	J5	52	S1
S2	J5	51	S2
S3	J5	50	S3
S4	J4	53	S0
S5	J4	52	S1
S6	J4	51	S2
S7	J4	50	S3
S8	J3	53	S0
S9	J3	52	S1
S10	J3	51	S2
S11	J3	50	S3
S12	J2	53	S0
S13	J2	52	S1
S14	J2	51	S2
S15	J2	50	S3
S16	J5	49	S4
S17	J5	48	S5
S18	J5	47	S6
S19	J5	46	S7
S20	J4	49	S4
S21	J4	48	S5
S22	J4	47	S6
S23	J4	46	S7
S24	J3	49	S4
S25	J3	48	S5
S26	J3	47	S6
S27	J3	46	S7
S28	J2	49	S4
S29	J2	48	S5
S30	J2	47	S6
S31	J2	46	S7

DAP 4400a Expansion Pin Mapping, continued
(OPTION AINEXPAND=ON)

DAPL Pin	Connector Number	Connector Pin	Termination Board Label
S32	J5	45	S8
S33	J5	44	S9
S34	J5	43	S10
S35	J5	42	S11
S36	J4	45	S8
S37	J4	44	S9
S38	J4	43	S10
S39	J4	42	S11
S40	J3	45	S8
S41	J3	44	S9
S42	J3	43	S10
S43	J3	42	S11
S44	J2	45	S8
S45	J2	44	S9
S46	J2	43	S10
S47	J2	42	S11
S48	J5	41	S12
S49	J5	40	S13
S50	J5	39	S14
S51	J5	38	S15
S52	J4	41	S12
S53	J4	40	S13
S54	J4	39	S14
S55	J4	38	S15
S56	J3	41	S12
S57	J3	40	S13
S58	J3	39	S14
S59	J3	38	S15
S60	J2	41	S12
S61	J2	40	S13
S62	J2	39	S14
S63	J2	38	S15

With `OPTION AINEXPAND=OFF`, the input pin mappings are as shown below:

Pin Group	Analog Expansion Pin Numbers
SPG0	S0 on each termination board
SPG1	S1 on each termination board
SPG2	S8 on each termination board
SPG3	S9 on each termination board
SPG4	S2 on each termination board
SPG5	S3 on each termination board
SPG6	S10 on each termination board
SPG7	S11 on each termination board
SPG8	S4 on each termination board
SPG9	S5 on each termination board
SPG10	S12 on each termination board
SPG11	S13 on each termination board
SPG12	S6 on each termination board
SPG13	S7 on each termination board
SPG14	S14 on each termination board
SPG15	S15 on each termination board

Index