DAP 820 Manual

Installation Guide and
Connector Reference

Version 1.00

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Contents

1. Introduction

The Data Acquisition Processor from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 820::

- has an onboard Intel 80C186XL processor
- samples data at up to 312K samples per second
- updates analog or digital outputs at up to 312K samples per second.
- transfers data to the PC at up to 312K samples per second.

The DAP 820 uses DAPL as the onboard operating system, which is optimized for the 16-bit processors used by these boards.

About This Manual

This manual includes hardware and software installation instructions and a hardware connector reference. Three other manuals provide information about creating data acquisition applications:

- The DAPL Manual contains a complete DAPL reference.
- The Applications Manual contains many useful examples of Data Acquisition Processor applications.
- The Systems Manual describes support software that runs in the PC, including support for writing programs that run in the PC.

2. Installation, Testing, & Troubleshooting

Installing a Data Acquisition Processor involves the following steps:

1. If necessary, change jumper settings on the Data Acquisition Processor.
2. Install the Data Acquisition Processor.
3. Install the DAP Software.
4. Test the Installation.

Installation instructions are provided in this chapter. Advanced installation information is provided in Chapter 3. If there are any problems with installation, please read the troubleshooting guide at the end of this chapter.

Data Acquisition Processor Handling Precautions

Static control is required for handling all electronic equipment. The Data Acquisition Processor is especially sensitive to static discharge because it contains many high-speed analog and digital components. To protect the Data Acquisition Processor, observe the following precautions:

- Wear a grounding strap when handling the Data Acquisition Processor. If it is not possible to use a grounding strap, continuously touching a metal screw on a grounded PC offers protection.
- If it is necessary to transport the Data Acquisition Processor outside of the PC, be sure to shield the Data Acquisition Processor in a conductive plastic bag. If a conductive bag is not available, shield the Data Acquisition Processor by wrapping it completely in aluminum foil. Do not ship or store a Data Acquisition Processor in plastic peanuts without suitable shielding.

Static damage to analog components can cause subtle problems, including oscillation, increased settling time, and reduced slew rate. If you suspect that a Data Acquisition Processor has been affected by static discharge, return it to Microstar Laboratories for testing, repair, and quality control.

System Requirements

The Data Acquisition Processor is compatible with 16-bit ISA or 32-bit EISA slots in AT/386/486/Pentium computers and requires version 3.0 or higher of DOS.

Standard Configurations

The Data Acquisition Processor is factory-configured to use interrupt 2 and I/O addresses in the range 220-22F (hexadecimal). This configuration does not conflict with most standard PC hardware. If you have nonstandard PC hardware or if any installed cards that use the same interrupt vector or I/O address as the Data Acquisition Processor, please read Chapter 3 before preceding with installation.

Note: Some sound cards are known to use I/O addresses in the 220-22F range. If your system has a sound card, check the configurations.

Interrupt and I/O address conflicts may cause subtle or obvious problems in your PC. After installing the Data Acquisition Processor, if your PC does not operate properly, check that there are no configuration conflicts.

Installing the Data Acquisition Processor

Caution: Do not install the Data Acquisition Processor while the PC is on.

To Install the Data Acquisition Processor:

1. Make any necessary changes to the hardware configurations.
Interrupt vector and I/O address information is provided in Chapter 2. Chapter 3 provides information about setting other hardware options. The default hardware settings are correct for most systems.
2. Turn off the PC and remove the PC's cover.
3. Insert the Data Acquisition Processor into any free PCI slot.

The Data Acquisition Processor requires approximately 15 Watts from the PC's power supply. If your system behaves erratically with the Data Acquisition Processor installed, the PC may need a larger power supply.

Installing DAP Software

Before installing the DAP Software, make backup copies of the diskette(s). Put the originals in a safe place, and use the backup disks for installation.

To Install Data Acquisition Processor Software:

1. Install the Data Acquisition Processor, as previously described.
2. Insert the DAP software disk into the PC's diskette drive.
3. At the DOS prompt, type `A:/INSTALL`.
4. Follow the on-screen instructions.

INSTALL prompts for configuration information including Data Acquisition Processor type and software destination directories. INSTALL provides information about each step to guide you through the installation process and provides options for copying DAPview and other software and Data Acquisition Processor support software to your PC.

INSTALL copies several files to your boot disk and adds information to your system configuration files `CONFIG.SYS` and `AUTOEXEC.BAT`. Backup copies of these files are created with the `.BAK` extension so that the original versions can be recovered.

Testing Installation

After running the INSTALL program, verify that software installation was successful by rebooting your PC. Before you see the DOS prompt, the following lines should appear on your screen:

```
ACCEL device driver 4.3
ACCEL driver initialization completed
DAPL initialization completed
```

The exact lines may vary slightly, depending upon configuration options. If a line is missing or if an error message appears, see the Troubleshooting section in this chapter.

When the DOS prompt is displayed, set the current directory to your DAPview directory and run DAPview by entering the following command:

```
DV
```

DAPview allows you to communicate interactively with the Data Acquisition Processor. Now everything you type at the PC keyboard is sent to the Data Acquisition Processor and all Data Acquisition Processor messages are printed on your screen. When the DAPview program begins, the following lines should be displayed on your screen:

```
*** DAPview [1.2] ***
*** DAPL Interpreter [4.XX XX/X] Serial# XXXXX ***
#
```

The appearance of the # prompt indicates that the Data Acquisition Processor is installed correctly. If the # prompt does not appear or if DAPview issues an error message and terminates, you have not established communication with the Data Acquisition Processor. Turn to the end of this chapter for troubleshooting hints.

Note: To exit from DAPview, press the Ctrl and Z keys simultaneously.

The number sign (#) indicates that the Data Acquisition Processor is waiting for a command. At this time you can enter DAPL commands from the keyboard or load DAPL command files. Sample applications are provided in the Applications Manual. The Systems Manual contains more information about DAPview.

Troubleshooting

The Systems Manual contains a list of the error messages which may be printed during software installation and system boot. The following errors commonly result from installation problems:

`INSTALL prints an error message.`
Find the error message in the "System Messages" chapter of the Systems Manual.

`At system startup, the "ACCEL device driver 4.3" message is not printed. OR`
`DAPview prints the error message "Host communication port is uninitialized"`
Check that the file `CONFIG.SYS` is present on your boot volume. If this file was not present before installation, it should have been placed on your boot volume by INSTALL. If the file `CONFIG.SYS` is present, check that it includes the line

```
DEVICE=x:\yyy\ACOM.SYS ...
```

The `"x"` character should be the letter of your boot disk. `"yyy"` should be the correct directory where the file `ACOM.SYS` is located. If `CONFIG.SYS` is not on your boot volume, or if the `ACOM.SYS` line of the file `CONFIG.SYS` is incorrect, use INSTALL again, being careful to install the software on the correct volume.

`The message "Bad or missing ACOM.SYS" is printed.`
The file `ACOM.SYS` probably was not copied by INSTALL from the Data Acquisition Processor diskette to your boot volume. Use INSTALL again, being careful to install the software on the correct volume.

`When your system is booted, one of the following messages is printed:`

```
DAP hardware not found or improperly configured
DAP interrupt conflict
DAP interrupt selection error
```

These messages suggest a hardware conflict with another card in the PC; one or more of the Data Acquisition Processor configuration jumpers may need to be changed to resolve the conflict. See Chapter 3.

`At system startup, the message “ACCEL driver initialization completed” is not printed.`

If an error message is printed by the ACOMINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command ACOMINIT. If no ACOMINIT line is found, use INSTALL again, being careful to install the software on the correct volume.

`At system startup, the message “DAPL initialization completed” is not printed.`

If an error message is printed by the DAPLINIT program, find the error message in the Systems Manual. If no error message is printed, check that the `AUTOEXEC.BAT` file on your boot volume contains a line beginning with the command DAPLINIT. If no DAPLINIT line is found, use the INSTALL pro-gram again, being careful to install the software on the correct volume.

`DAPview issues the error message “Could not establish communi-cations” OR DAPview does not display a DAPL # prompt.`

The Data Acquisition Processor is not communicating with your PC. This may indicate that an error occurred at boot time. Check that no error messages are printed when you boot your system.

If your PC has cards other than those listed at the beginning of the chapter, a card may be interfering with communications. Remove optional cards, boot the PC, and try using DAPview again.

Check that the configuration jumpers on the Data Acquisition Processor are correct. See Chapter 3 for the correct jumper selections. Check also for consistency between the jumper settings and the settings on the `ACOM.SYS` line in the file `CONFIG.SYS`.

A final possibility is that the Data Acquisition Processor may be faulty. If you suspect that this is the case, call Microstar Laboratories. When calling for installation support, please open your PC case so that the Data Acquisition Processor jumpers are visible, and be ready to provide the following information:

- the serial and model numbers of your Data Acquisition Processor.
- the contents of your `AUTOEXEC.BAT` and `CONFIG.SYS` files.
- a list of all hardware boards installed in your computer.

`Your PC keyboard locks up when DAPview is started and does not accept the Ctrl-Z key.`

Your PC may have an old style keyboard. Try starting DAPview with one of the following command line options:

```
DV /K1
DV /K2
```

`DAPview issues the error "Help file DV.HLP not found."`

Check that the file `DV.HLP` has been copied to the directory containing the DAPview files. Check also to make sure the file `AUTOEXEC.BAT` has the line:

```
SET DV=C:\DV
```

Replace `C:\DV` with the drive and directory containing the `DV.HLP` file.

3. Advanced Installation Options

Installation for standard hardware configurations is described in Chapter 2. This chapter covers installation in more detail.

Nonstandard Configurations

The Data Acquisition Processor uses two resources from the host PC:

- an interrupt vector
- a range of I/O addresses

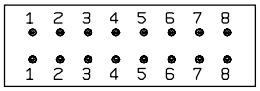
The Data Acquisition Processor allows several interrupt vector and I/O address selections. The interrupt vector may be 2, 3, 4, or 5. When selecting an interrupt vector, note the following interrupt vectors used by standard cards:

EGA/VGA	2
serial port COM2	3
serial port COM1	4
parallel port #2	5
hard disk controller on IBM XT	5
parallel port #1	7

The Data Acquisition Processor is shipped configured to use interrupt 2. EGA and VGA video adapters potentially can use interrupt 2, but most applications do not use this capability. Since interrupt 2 does not conflict with any other standard hardware, this is the default Data Acquisition Processor interrupt vector.

If any other cards are installed, determine the interrupts used and select a Data Acquisition Processor interrupt number distinct from these. Depending on the selection, the host computer may lose access to one of the serial COM ports or one of the parallel ports.

To change interrupt vectors, locate the 16-pin `HOST CONFIGURE` connector:



J10 HOST CONFIGURE

Connector J10 is directly above the gold fingers on the Data Acquisition Processor printed circuit board.

The following table gives the four possible interrupt selections:

Interrupt Vector	Jumper
2	pin pair 7
3	pin pair 4
4	pin pair 5
5	pin pair 6

To change the interrupt, remove the jumper and replace it according to this table. Note that exactly one of the pin pairs 4, 5, 6, and 7 should be connected.

When the interrupt is changed, the INSTALL program must be informed of the new interrupt selection. When running INSTALL, select the `DAP 0` button and select the interrupt number that matches the interrupt of the Data Acquisition Processor.

In addition to an interrupt vector, the Data Acquisition Processor uses a range of I/O addresses. If a sound card or any nonstandard cards are used in the host PC, check that the Data Acquisition Processor I/O addresses do not conflict with those cards.

The Data Acquisition Processor is shipped configured to use I/O addresses in the range 220-22F (hexadecimal). This range may be changed by changing the jumpers on the `HOST CONFIGURE` connector. Pin pairs 1, 2, and 3 select the I/O address of the Data Acquisition Processor according to the following table:

I/O Address Range	Jumpers
220 - 22F	1, 2, 3
230 - 23F	2, 3
240 - 24F	1, 3
250 - 25F	3
320 - 32F	1, 2
330 - 33F	2
340 - 34F	1

When the I/O address is changed, the INSTALL program must be informed of the new address selection. When running INSTALL, select the `DAP 0` button and select the address that matches the address of the Data Acquisition Processor.

Note: The only effect of changing the interrupt number or address in the INSTALL program is to change the value of the `/I` or `/A` parameter of the line `ACOM.SYS` that is inserted in the file `CONFIG.SYS`.

The INSTALL Program

This section provides additional details about the INSTALL program. This information is of interest only to advanced Data Acquisition Processor users.

The INSTALL program installs Data Acquisition Processor software on a PC and configures the PC to initialize the ACCEL driver when the PC boots. INSTALL uses the following syntax:

```
A: INSTALL <options>
```

If installing from a drive other than `A:`, type the letter for that drive instead. INSTALL allows several command line options for special installation features. The following options are legal:

`/COMx`	Use serial port communication on com port x (DAP 801 only)
`/Mxx`	Default ACCEL driver mode (See the Systems Manual)
`/Dx`	Install more than one DAP
`/?`	Help

When running INSTALL, several prompts are provided for configuring Data Acquisition Processor software on a PC. Select a DAP button to choose the DAP model, address, and interrupt for the Data Acquisition Processor. Choose the Select Software Options button to select the specific software options to install. For help on the options press F1.

After all options have been verified, INSTALL copies Data Acquisition Processor software to the PC and modifies the system files. INSTALL copies the files `ACOM.SYS`, `ACOMINIT.EXE`, `DAPLINIT`, and `Dx-x.STD` to the PC boot drive. INSTALL creates the file `ACOM.DAT` and places it on the boot drive. These files are all placed on the boot drive so they are available when the PC first boots.

After copying the boot files, INSTALL copies the software that was specified in the Select Software Options dialog box to the Main directory.

INSTALL adds a line to the file `CONFIG.SYS` that loads the ACCEL device driver. If this line already exists from a previous installation, INSTALL replaces it. The following line is a typical line that INSTALL adds to `CONFIG.SYS`:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

More information about the ACCEL driver configuration line is provided later in this chapter. If `CONFIG.SYS` does not exist, INSTALL creates it. Before modifying `CONFIG.SYS`, INSTALL saves an original copy in the file `CONFIG.BAK`.

INSTALL also modifies the file AUTOEXEC.BAT by adding several lines that configure the ACCEL driver with specific communication information. If these lines already exist from a previous installation, INSTALL replaces them. The following lines are typical lines that INSTALL adds to AUTOEXEC.BAT:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

The ACOMINIT program configures the ACCEL driver with specific communication pipe information provided by the file ACOM.DAT. For some Data Acquisition Processor models, the DAPLINIT program is required to initialize the DAPL operating system. More information about the ACOMINIT and DAPLINIT programs is provided later in this chapter. If AUTOEXEC.BAT does not exist, INSTALL creates it. Before modifying AUTOEXEC.BAT, INSTALL saves an original copy in the file AUTOEXEC.BAK.

Device Driver Configuration

This section explains the format of the device driver command that is placed in the `CONFIG.SYS` file by the INSTALL program. This information is of interest only to advanced programmers.

The format of the device driver command is:

```
DEVICE=ACOM.SYS [Ix] [DAP[yyy]:Azzz] [Muu] [Pwww]
```

Note: Several parameters are optional. The letters u through z in each parameter represent hexadecimal digits.

`x` specifies the interrupt vector that is used for PC communication. This number should match the configuration of jumper `J10` on the Data Acquisition Processor.

The ACCEL driver automatically detects the type of Data Acquisition Processor that is installed. `yyy` is optional and manually specifies the board type. For the DAP 820, `yyy` is `820`.

`zzz` specifies the hexadecimal starting I/O address of the Data Acquisition Processor. This number must match the configuration of jumper `J10` on the Data Acquisition Processor.

`uu` is a hexadecimal number that specifies the default mode of the ACCEL driver. See the Systems Manual for more information about ACCEL driver modes.

`www` is a hexadecimal number that specifies the number of paragraphs of memory to reserve for PC communications pipes. See “Com Pipe Configuration” later in this chapter.

The following is a typical ACCEL driver command line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

The ACCEL driver can be loaded into high memory with the DOS `devicehigh` statement. See your DOS manual for details on loading device drivers into high memory.

The ACOMINIT Program

ACOMINIT configures the ACCEL driver communication pipes. ACOMINIT is placed in the file `AUTOEXEC.BAT` to configure the ACCEL driver when the PC first boots. The syntax for ACOMINIT is:

```
ACOMINIT <cfg_file>
```

`<cfg_file>` provides communication pipe configuration information. `<cfg_file>` normally is named `ACOM.DAT`. The following section describes the contents of `ACOM.DAT`.

Com Pipe Configuration

This section describes the format of communication pipe configuration in the file ACOM.DAT. This information is not required for most applications. During initialization, the Microstar Laboratories program ACOMINIT reads the contents of a configuration file which specifies a com pipe configuration. The configuration file determines the connection between com pipes on the Data Acquisition Processor and com pipes on the PC. Lines in the configuration file have the following syntax:

```
<source> -> <destination> [<options>]
```

<source> and <destination> are specifications of communication pipe locations. A com pipe location is either a Data Acquisition Processor com pipe, a PC com pipe:

```
(DAP[n] CPIPE v)
(PC CPIPE w)
```

n is the Data Acquisition Processor number when several boards are installed in one PC. v is a DAPL com pipe number, w is a PC com pipe number. The space before v and w can be omitted.

For example, the following lines connect the default text input and text output com pipes of the Data Acquisition Processor to the PC:

```
(dap cpipe 0) -> (pc cpipe 0)
(pc cpipe 0) -> (dap cpipe 0)
```

The first line connects DAPL output com pipe 0 to PC input com pipe 0. The second line connects PC output com pipe 0 to DAPL input com pipe 0. By default, DAPL defines two input com pipes and two output com pipes. Output com pipe 0, named $SYSOUT, is for text output to the PC. Output com pipe 1, named $BINOUT, is for binary output to the PC. Input com pipe 0, named $SYSIN, is for text input from the PC. Input com pipe 1, named $BININ, is for binary input from the PC.

Each line in the com pipe configuration file may contain one or more options, enclosed in square brackets. The following options are available:

```
BINARY|TEXT
MAXSIZE=xx
WIDTH BYTE | WORD | LONG
```

BINARY and TEXT specify the type of the data in the com pipe. The default is TEXT.

MAXSIZE specifies the size of the PC buffer of the com pipe, in bytes. The default is 1024 bytes. The INSTALL program sets the maximum size of the com pipes to be relatively small to conserve PC memory yet provide good performance. The Data Acquisition Processor automatically provides additional pipe buffering when needed. In some applications, increasing the maximum com pipe size can improve performance by allowing larger block operations. Performance can increase with com pipe sizes up to 4096 or 8192. Larger com pipe sizes typically do not provide further performance benefits.

WIDTH specifies the width of data items that are transferred through the com pipe. The WIDTH option must match the width of the corresponding Data Acquisition Processor com pipe. BYTE is the default for text com pipes and also is the only width allowed. WORD is the default for binary com pipes. Any width is allowed for binary com pipes.

The default com pipe configuration file generated by the INSTALL program is stored in the file ACOM.DAT. If the Data Acquisition Processor is operated inside a PC, the following configuration is placed in the file ACOM.DAT:

```
(dap0 cpipe0) -> (pc cpipe0) [text maxsize=1024]
(pc cpipe0) -> (dap0 cpipe0) [text maxsize=1024]
(dap0 cpipe1) -> (pc cpipe1) [binary maxsize=2048]
(pc cpipe1) -> (dap0 cpipe1) [binary maxsize=1024]
```

In some applications, additional com pipes need to be defined. More com pipes are needed when extra com pipes are defined in DAPL on a Data Acquisition Processor or when several Data Acquisition Processors are installed.

For special applications, extra com pipes can be defined in DAPL. See the CPIPE command in the DAPL Manual.

Note that in many cases, the commands MERGE, MERGEF, and NMERGE can be used instead of defining extra com pipes. It is best to use standard com pipes when possible to maintain a standard communication setup.

When more than one Data Acquisition Processor is installed in a system, additional com pipes need to be defined. For several Data Acquisition Processors, the following com pipe numbering is recommended:

```
DAP0
   system text pipe is PC com pipe #0
   system binary pipe is PC com pipe #1
DAP1
   system text pipe is PC com pipe #2
   system binary pipe is PC com pipe #3
 .
 .
DAP6
   system text pipe is PC com pipe #12
   system binary pipe is PC com pipe #13
```

P Parameter Size

In a system with additional com pipes, the memory available to the ACCEL driver must be increased. The `P` parameter in the `ACOM.SYS` line of the file `CONFIG.SYS` specifies the number of paragraphs of PC memory reserved for the ACCEL driver and com pipes. The storage requirement of the ACCEL driver and PC com pipes, in bytes, is:

```
storage = 830 + (maxsize in bytes) + (number of com
pipes)*190
```

`MaxSize in bytes` is the sum of all com pipe sizes defined in the file `ACOM.DAT`. `Number of com pipes` is the number of com pipes defined.

Note: This storage requirement applies for version 4.34 of the ACCEL driver. Subsequent driver versions may require additional storage.

The `P` parameter is a hexadecimal number, specified in paragraphs. A paragraph of PC memory is 16 bytes. To determine the `P` parameter, divide the storage requirements by 16 and convert to hexadecimal.

The following example calculates the `P` parameter for the default `ACOM.DAT` file created by INSTALL. The result, in bytes, is divided by 16 to get the `P` parameter in paragraphs.

```
storage = 830 + 5120 + 4*190 = 6710 bytes
p= 6710/16 = 420 paragraphs (decimal) = 1A4 (hex)
```

When defining additional com pipes, remember to define pipes for both the DAP-to-PC and PC-to-DAP direction. Some programs such as DAPview for Windows expect additional com pipes defined for both directions.

DAP-to-DAP Communication

Communication pipes can be configured to allow communication between two Data Acquisition Processors. DAP-to-DAP communication occurs over the PC bus in the background with no PC program intervention required. The following syntax is used in the file ACOM.DAT to configure DAP-to-DAP communication:

```
(DAPw CPIPEx) -> (DAPy CPIPEz)
(DAPy CPIPEz) -> (DAPw CPIPEx)
```

w is the number of the DAP that sends data. x is the DAP communication pipe used to send data. y is the number of the DAP that receives data. z is the DAP communication pipe to receive data. The DAPL command CPIPE is needed to define the DAP communication pipes on each DAP.

The following example shows how to configure a system for DAP-to-DAP communication. This example configures two DAPs. DAP 0 samples one channel of data and sends the data to DAP 1 for analog output.

In the file ACOM.DAT, add:

```
(dap0 cpipe15) -> (dap1 cpipe15)   [binary maxsize=1024]
(dap1 cpipe15) -> (dap0 cpipe15)   [binary maxsize=1024]
```

DAP-to-DAP com pipes require twice the storage space as DAP-to-PC or PC-to-DAP com pipes. For the above DAP-to-DAP com pipe definition, the P parameter in CONFIG.SYS must be increased by 130 (hex). The following example calculates the P-parameter increase:

```
storage increase= 2 * (2048 + 2 * 190) = 4856 (decimal)
p increase=4856/16 = 304 paragraphs (decimal) = 130 (hex)
```

The following DAPL commands provide an example of how to implement DAP-to-DAP communication.

```
;  DAPL commands for DAP 0:
CPIPE TODAP1 PC NUM=15 OUTPUT BINARY WORD
RESET
IDEF A 1
   SET IPIPE S0
   TIME 10000
   END
PDEF B
   COPY(IPIPE0, TODAP1)
   END
START A,B

;  DAPL commands for DAP 1:
CPIPE FROMDAP0 PC NUM=15 INPUT BINARY WORD
RESET
PDEF A
   COPY(FROMDAP0, $BINOUT)
   END
START A
```

The DAPLINIT Program

DAPLINIT initializes the DAPL operating system on the Data Acquisition Processor by downloading a binary image of DAPL to the Data Acquisition Processor. ACCEL driver communication pipes must be configured using ACOMINIT before DAPLINIT is run. The syntax for DAPLINIT is as follows:

```
DAPLINIT [/RESET] [<dapl_file>] [<dapl_file>]*
```

`<dapl_file>` specifies a binary file containing DAPL. DAPLINIT allows several DAPL binary files to initialize several Data Acquisition Processors in a PC.

The optional parameter `/RESET` requests a hardware reset of the Data Acquisition Processor before downloading DAPL. If `/RESET` is not specified, all Data Acquisition Processors retain their state during a warm PC boot.

DAPLINIT detects the Data Acquisition Processor model types on the `ACOM.SYS` line of the file `CONFIG.SYS`. DAPLINIT downloads the DAPL files, in order, to the Data Acquisition Processors that require DAPL initialization.

DAPLINIT can accept a wildcard file specification to allow flexibility for when DAP installations change. With a wildcard file name, DAPLINIT searches the current directory and the DOS PATH to find a DAPL binary file that matches the DAP type that is installed. The following example shows how DAPLINIT can be configured to search for the correct `DAPL/STANDARD` binary file.

```
DAPLINIT /RESET D*.STD
```

The INSTALL program automatically configures new installations to use a wildcard file name for DAPLINIT.

Installing Several Data Acquisition Processors

Up to seven Data Acquisition Processor boards can operate simultaneously in one PC. Running several boards in parallel increases the maximum sampling rate and the real-time processing power of a system. For special options to install up to 14 Data Acquisition Processor boards in one PC, contact Microstar Laboratories.

Each Data Acquisition Processor requires one PC slot. All the Data Acquisition Processors in a PC share just one interrupt line; no DMA lines are required. The Data Acquisition Processors are distinguished by their I/O addresses in the PC. Before installing Data Acquisition Processors in the PC, select a distinct I/O address for each board.

There are seven possible I/O addresses; this limits the number of Data Acquisition Processors in a PC to seven. Set the I/O addresses with the jumpers on the `HOST CONFIGURE` connector. Information about the `HOST CONFIGURE` connector is provided at the beginning of this chapter.

Note: Pin pair 8 of the `HOST CONFIGURE` connector sets the level of the PC's interrupt line. Pin pair 8 must be connected for one Data Acquisition Processor in a PC, and must not be connected for all other Data Acquisition Processors.

INSTALL can perform installation for several Data Acquisition Processors. When typing the INSTALL command, add the option `/Dx` to the end of the command, where `x` is the number of boards. For example, the following line defines installation for three Data Acquisition Processors.

```
A:INSTALL /D3
```

INSTALL provides on-screen options for configuring each Data Acquisition Processor individually. Select a DAP button to display a dialog box for choosing the Data Acquisition Processor model, address, and interrupt.

Note: The order in which the boards appear in the `ACOM.SYS` line in the file `CONFIG.SYS` determines the numbering of the Data Acquisition Processors. The first Data Acquisition Processor is `DAP 0`, the second is `DAP 1`, etc. The addresses do not matter when determining the numbering. When synchronous operation is used with DLOG, the last board in the list is the master unit.

Installation on a Network

Data Acquisition Processor software can be installed on a network consisting of PC workstations connected to one or more servers. The INSTALL program can copy Data Acquisition Processor software to a PC workstation from a network that has a copy of the DAP Software disk image.

Note: When using Data Acquisition Processor software on a network, each simultaneous user must have a licensed copy of the software.

When installing Data Acquisition Processor software from a network, INSTALL copies several files to the PC workstation boot drive. The files are `ACOM.SYS`, `ACOMINIT.EXE`, `ACOM.DAT`, and, if necessary, `DAPLINIT.EXE` and `Dx-x.STD`. These files must be on the PC boot drive so that they are available immediately at boot time. INSTALL copies the remaining Data Acquisition Processor software to a network drive for use once the network is connected. INSTALL modifies `AUTOEXEC.BAT` and `CONFIG.SYS` on the workstation boot drive as in regular installations.

DAPL Licensing

When a Data Acquisition Processor is shipped from the factory, a copy of DAPL is provided that is licensed to run on the Data Acquisition Processor. When a DAP Software Upgrade is shipped, the DAPL file on the upgrade is licensed to be used with the Data Acquisition Processor that was specified when the upgrade was ordered.

Removing Data Acquisition Processor Software

When a Data Acquisition Processor is removed from a PC, the software can be removed as well. This section describes how to remove a Data Acquisition Processor software installation.

1. Delete the directory where Data Acquisition Processor software was in-stalled. Usually this directory is `c:\dap`. Delete all the subdirectories under the DAP directory. Make sure that there are no important data files in these directories before deleting them.

2. Edit the file `AUTOEXEC.BAT`. Delete the four lines that match the following four lines:

```
c:\dap\acominit c:\dap\acom.dat
@if errorlevel 1 pause
c:\dap\daplinit /reset c:\dap\d*.std
@if errorlevel 1 pause
```

3. Edit the file `CONFIG.SYS`. Delete the line that matches the following line:

```
device=c:\dap\acom.sys i2 dap:a220 m20 p1A4
```

4. DAP 820 Connectors

This chapter discusses the interface connectors on the DAP 820. Diagrams and documentation for input/output connector, the output clock connector, and jumpers the are provided in this chapter.

Detailed instructions for setting the following options are provided in this chapter:

- the analog input voltage range (J7, J8)
- the output voltage ranges of DAC0 and DAC1 (J11 and J12)
- the digital output polarity at power-on (J32)
- input/output synchronization (J22)

Figure 1 shows component placement outlines of the DAP 820. The only components shown are connectors, whose labels begin with the letter J, some integrated circuits, whose labels begin with the letter U, and trim potentiometers, whose labels are single letters.

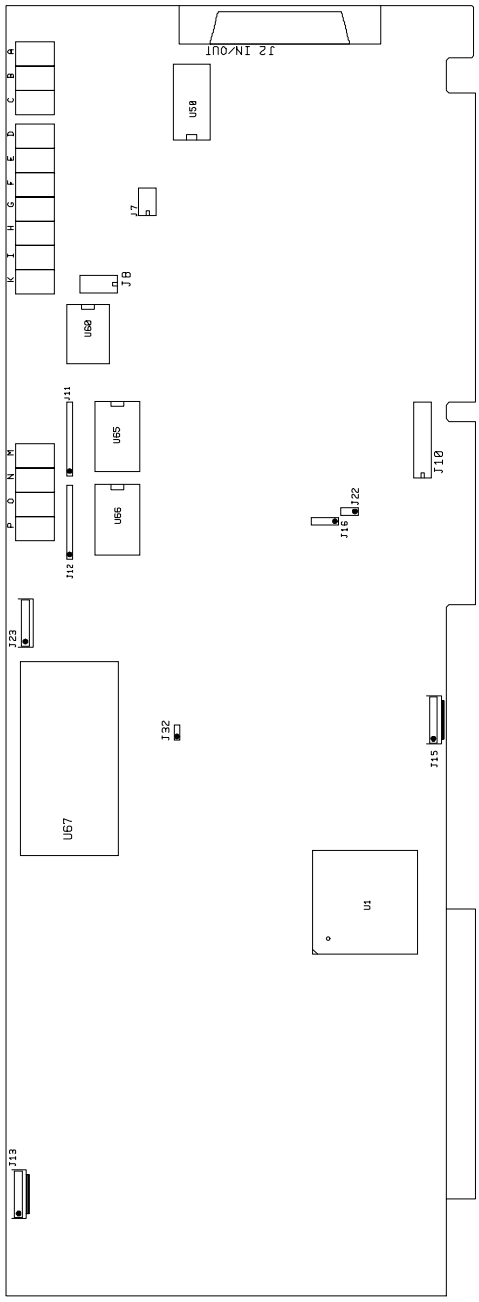
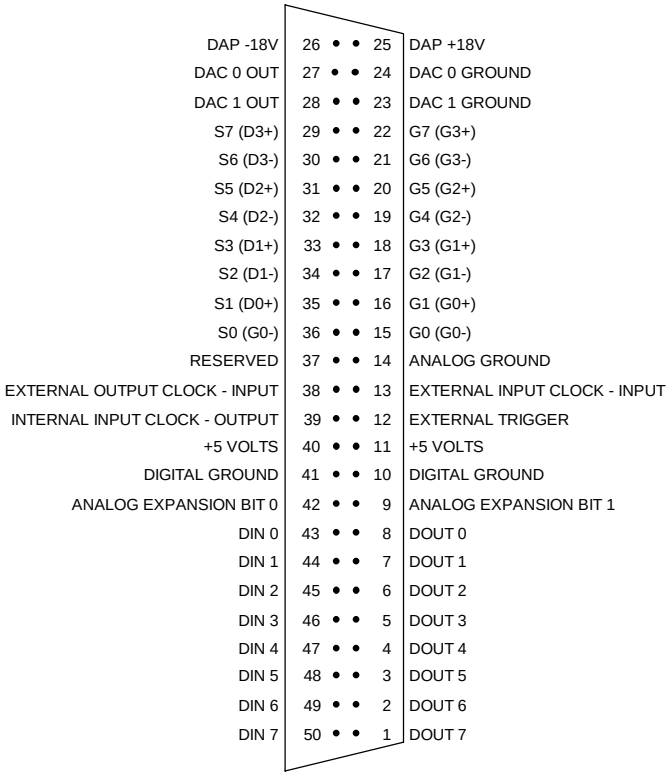


Figure 1. DAP 820

Input/Output Connector

Analog and digital voltages are connected to the Data Acquisition Processor through a 50-pin connector on the back panel of the PC. This connector is located on the right side of the Data Acquisition Processor and is labeled `J2 IN/OUT`. It has a double row of pins on 0.050 inch centers. The connector is AMP part number 749649-5. This connector mates with discrete wire connector T&B part number HFM050A or insulation displacement connector AMP part number 786090-5. J2 mates with cable part numbers MSCBL 047-01, MSCBL 048-01, MSCBL 049-01K, MSCBL 050-01, and MSCBL 051-01K.

Looking at the input/output connector from the back of a PC, the pin numbering is:



Note: Use the pin numbering on this chart, rather than numbers which may be found on your connector. Connectors from different manufacturers are not numbered consistently.

Single-ended analog inputs are indicated by S0 through S7; their corresponding ground inputs are G0 through G7. Differential inputs are indicated by D0- and D0+ through D3- and D3+; their corresponding ground inputs are G0- and G0+ through G3- and G3+.

Digital inputs are indicated by DIN 0-7 and digital outputs are indicated by DOUT 0-7. Bit 0 is the least significant bit.

Digital-to-analog outputs are indicated by DAC0 and DAC1. Their corresponding ground returns are DAC0 GROUND and DAC1 GROUND.

Pin 13 is the external input clock input and pin 39 is the internal input clock output. Pin 12 is the external input trigger connection. Pin 38 is the external output clock input.

Pins 11 and 40 are connected to the 5-volt digital power supply. Pins 25 and 26 are +18-volt and 18-volt supplies respectively.

Pins 37 is reserved and should not be used.

A termination board that connects all lines of the input/output connector to discrete wire connectors is available from Microstar Laboratories. See Chapter 7 for a description of the DAP 820 Termination Board.

The following sections describe the input/output connector pins in greater detail.

Analog Input

Analog voltages are connected to the DAP 820 through the 50-pin input/output connector on the back panel of the PC. See the previous section for the input/output connector pinout.

A single-ended analog signal should be connected to an analog input pin and to the adjacent analog ground pin, for example to pins 36 and 15. A differential analog signal should be connected to two adjacent analog input pins and to either of their corresponding grounds, for example to input pins 36 and 35, and ground pin 15 or ground pin 16.

Analog input signals should be within the range from -10 volts to +10 volts, relative to the ground of the Data Acquisition Processor. The DAP 820 is provided with fault-protected input multiplexers. The analog inputs are protected against voltages up to ±25 volts. Input signals within this range may be applied to the DAP 820 when the PC's power is off.

Analog Output

The input/output connector on the DAP 820 includes digital-to-analog converter outputs. Pins 27 and 28 are the outputs of `DAC0` and `DAC1`, respectively. Pins 24 and 23 are the corresponding grounds. The digital-to-analog converters have voltage outputs with typical output impedances of 2 Ohms. These normally should drive high impedance inputs. The output current from each digital-to-analog converter output is rated at ±5 milliamps but it is recommended that this current not exceed ±1 milliamp.

Analog outputs are set to zero when the system is first powered on. When analog outputs are configured for unipolar mode, the outputs are set to half of the full scale range when the system is first powered on. When J32 is moved, the analog outputs at power-on may vary by up to 5 millivolts.

Digital Input/Output

Digital input and output pins are located on the input/output connector on the back panel of the PC.

Digital inputs are indicated by `DIN 0-7` and digital outputs are indicated by `DOUT 0-7`. Bit 0 is the least significant bit.

The digital inputs are FCT TTL; they sink no more than 20 microamps for a “1” input and source no more than 0.2 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”. Each digital input has a 10 KΩ resistor to +5 volts.

Digital inputs may have signals applied when the Data Acquisition Processor is off.

Digital outputs are set to "0" when the system is first powered on. The digital outputs are FCT TTL; they can sink no more than 12 milliamps for a “0” output and can source no more than 2.6 milliamps for a “1” output. The output voltage for a “1” is at least 2.4V and the output voltage for a “0” is at most 0.55V.

External Clock and Trigger

The input/output connector on the DAP 820 includes connections for internal clock output, external clock input, and external trigger input.

The external input clock—input pin is used to connect an external input clock to the DAP 820. The internal input clock—output pin is the buffered output of the DAP 820 input clock circuit.

Pin 12 is an external trigger connection. The external trigger for the DAP 820 is either one-shot or gated, depending on the `HTRIGGER` command in the active input procedure. The external trigger of the DAP 820 is ignored if there is no `HTRIGGER` command in the active input procedure.

An external trigger signal must be within the standard TTL logic range of 0 to +5 volts. The Data Acquisition Processor provides a pull-up resistor on the external trigger input. This forces the trigger input active if it is left unconnected.

Clock and trigger inputs may have signals applied when the Data Acquisition Processor is off. See Chapter 6 for more information about the external clock and the trigger.

Supply Voltages

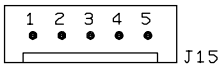
The input/output connector provides connections to DAP 820 supply voltages. Pins 25 and 26 are connected to +18 volt and -18 volt analog supplies. These supplies can be used for low current, low noise devices such as external multiplexers. The maximum allowable current drain from these supplies is 20 milliamps per side. If more current than this is required, either use an external supply or use the 5 volt digital power supply found on pins 11 and 40. The 5V supply has two connections on the Input/Output Connector, the output current is rated at 500 milliamps per connection.

Output Clock Connector

Connector J15 is a five-pin connector, Molex part number 22-23-2051; the mating connector is Molex part number 22-01-3057. J15 is located on the lower edge of the Data Acquisition Processor, between the 80186 CPU and the gold edge fingers.

The output clock signals and the output trigger signal are available on connector J15, along with power and ground. These signal pins can be used to control when outputs are updated.

The pin numbering for J15 is given in the following table:



Pin 1 Ground
Pin 2 External output trigger – input
Pin 3 Internal output clock – output
Pin 4 External output clock – input
Pin 5 +5 volts

Shunts

Several of the Data Acquisition Processor options are set by shunts. These are jumper wires enclosed in plastic, designed for connecting pins on 0.100" centers.

Each shunt has a top and a bottom. When a shunt is placed correctly, a probe point is visible in the shunt. Shunts must not be placed upside down on the pins, as incorrectly placed shunts do not provide reliable contacts.

Analog Signal Path Selection

In addition to the DAPL configuration options, the Data Acquisition Processor has several hardware configuration options. These determine the path taken by analog signals from the input pins to the analog-to-digital converter.

The analog signal path between the input pins and the analog-to-digital converter consists of the following functional units:

1. input multiplexers
2. instrumentation amplifier
3. programmable gain amplifier
4. bipolar offset circuit amplifier
5. analog-to-digital converter with sample-and-hold amplifier

Analog signals must pass through the input multiplexers, the instrumentation amplifier, and the analog-to-digital converter. Jumpers determine whether the analog signal path includes the programmable gain amplifier and the bipolar offset circuit, and also determine the input voltage range.

A signal range is called bipolar if it includes both positive and negative voltages; a signal range is called unipolar if it includes voltages of only one sign. The range amplifier allows the bipolar analog-to-digital converter to operate with unipolar voltages. Jumpers select from three bipolar ranges and one unipolar range. If the programmable gain amplifier is enabled, gains of 1, 10, 100, and 500 are software selectable.

Analog Signal Path Configuration

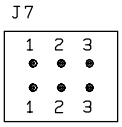
Two connectors control the analog signal path of the DAP 820. Note that changing voltage ranges may require recalibration.

The following table summarizes the DAP 820 analog input jumper connections:

ADC Range	J7	J8
0v to 5v	2	1-8, 3-6
±5v*	1 *	3-6, 4-5 *
±10v	2	3-4, 5-6

* Factory Configuration

The input signal to the bipolar offset circuit is selected by J7:

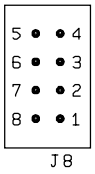


Exactly one jumper should be placed on J7, as follows:

Jumper	Signal range
1	unipolar
2	bipolar, gain enabled
3	bipolar, gain disabled

The unipolar input range is from 0 to +5 volts.

The input signal to the analog-to-digital converter is selected by `J8,` which selects the input voltage range as well as enabling or disabling gain if in bipolar mode. It is often desirable to leave gain enabled, even if only a gain of 1 is used.



Exactly two jumpers should be placed on J8, as follows:

Jumpers	Signal range
1-8, 3-6	unipolar, 0 to 5 Volts
4-5, 3-6	bipolar, ±5 Volts, gain enabled
2-7, 3-6	bipolar, ±5 Volts, gain disabled
3-4, 5-6	bipolar, ±10 Volts, gain enabled
3-4, 6-7	bipolar, ±10 Volts, gain disabled

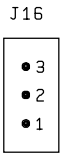
Note that jumpers on J8 may be placed horizontally or vertically.

Note: Regardless of the input voltage range, positive and negative differential signals may range from -10 volts to +10 volts.

Channel List Selection

The DAP 820 has two possible external input clocking modes. When Channel List Clocking is enabled, all input pins are sampled on each low to high transition of the external clock. When Channel List Clocking is disabled, a single pin is sampled on each low to high transition of the external clock.

Connector J16, located above the left-most gold edge connector, determines the clocking mode for external clocking. J16 is a three pin vertical header of one column on 0.100 inch centers. The factory configuration is “enabled.”

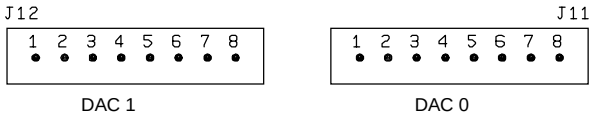


Exactly one jumper should be placed on `J16`, as follows:

Pins	Channel List Clocking
2, 3	disabled
1, 2	enabled

Analog Output Voltage Range Selection

The voltage ranges of DAC0 and DAC1 are selected by headers J11 and J12, respectively:



Three jumpers should be placed on J11 and J12, as follows:

Jumpers	Range
3 to 4, 5 to 6, 7 to 8	0 volts to +10 volts
1 to 2, 4 to 5, 7 to 8	-5 volts to +5 volts
1 to 2, 4 to 5, 6 to 7	-10 volts to +10 volts

Note: By default, DAPL assumes that the outputs of the digital-to-analog converters are bipolar. If a unipolar output range is selected, the following DAPL command must be issued:

```
OPTION BPOUTPUT=OFF
```

Digital Output Reset Polarity Jumper

The digital output reset polarity jumper J32 has two pins spaced at 0.100". J32 is located near the center of the Data Acquisition Processor, approximately 2.5" above J15. The digital output reset polarity jumper allows selection of the digital output polarity at power-on. If J32 is installed, all digital outputs will be reset to 0 at power-on. If J32 is removed, all digital outputs will be preset to 1 at power-on. All Data Acquisition Processors are shipped from the factory with J32 installed. The voltage of the analog outputs at reset may vary by up to 5 millivolts when J32 is removed.

Input/Output Synchronization Header

The input/output synchronization header J22 has two pins spaced at 0.100". J22 is located approximately one inch above the left set of gold fingers on the Data Acquisition Processor. If a shunt is placed on J22, the input trigger is connected to the output update clock. This causes a hardware input trigger to occur when an output procedure initiates its first update. This is used to synchronize input sampling to output updates.

Synchronization Connector

The synchronization connector `J13` has a single row of pins on 0.100 inch centers. `J13` is located at the upper left of the Data Acquisition Processor printed circuit board. The synchronization connector allows several Data Acquisition Processors to share the same sampling clock. See the Systems Manual for more information about using synchronous Data Acquisition Processors.

For synchronization, the shared sampling clock requires special cabling between Data Acquisition Processors. The analog sampling clock of the master unit is supplied to the slave units by means of the cable MSCBL 015-01. Contact Microstar Laboratories for more information about cabling for synchronous Data Acquisition Processors.

5. Analog Input Circuits

The analog input hardware of the Data Acquisition Processor is discussed in some detail in this chapter. The following summary gives sufficient information for most Data Acquisition Processor applications:

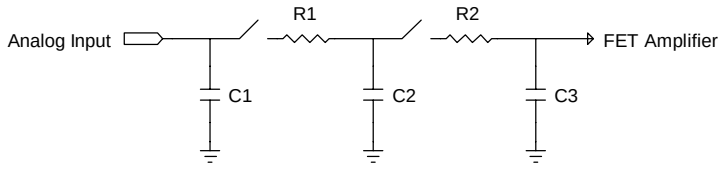
- The DC input impedance is very high.
- At high sampling rates, the signal source impedance should be low.
- Minimum sampling times are specified for unity gain.
- At gain 10, the fastest sampling rate is slower than the fastest sampling rate at gain 1.
- At gain 100 and 500, the fastest sampling rate is substantially slower than the fastest sampling rate at gain 1.

Analog Input Circuits

Data Acquisition Processor analog input signals pass through two analog multiplexers and then to an op amp with a FET input. The DC input impedance is very high, typically far in excess of 10M Ohms. The AC input impedance is dominated by the capacitance of the multiplexers.

Figure 2 shows a useful equivalent circuit for each Data Acquisition Processor input. As the Data Acquisition Processor scans through the input pins defined by an input procedure, the switches in the multiplexers open and close, connecting the specified inputs to multiplexer outputs. When an input signal is connected to the FET amplifier, the signal source must supply sufficient current to charge the equivalent capacitance of the multiplexers before the analog-to-digital conversion can start.

Figure 2



The DAP 820 has fault-protected multiplexers. The following table shows typical resistance and capacitance values, in Ohms and picofarads, for fault-protected multiplexers.

Component	Value
R1	300Ω
R2	100Ω
C1	5 pF
C2	55 pF
C3	30 pF

Programmable Gain Amplifier

At gains other than unity, the programmable gain amplifier requires extra time to switch from pin to pin and then settle to full accuracy. The following table shows typical minimum sampling times for each Data Acquisition Processor at each gain.

Minimum Sample Times in µS at Gain:

	1	10	100	500
DAP 820/103	3.20	8	40	500

6. Clocks and Triggers

The Data Acquisition Processor is designed to operate using either internal clocks or external clocks. The Data Acquisition Processor has onboard crystal-controlled timers to provide an internal input sampling rate and output update rate, and also has provisions for external clocks for both input and output.

The Data Acquisition Processor has hardware control lines for an input clock, an output clock and an input trigger. These lines all are TTL compatible. The input clock and the output clock both are positive-edge triggered.

The input clock on all models has two modes. In the first mode, called Channel List Clocking, the Data Acquisition Processor starts conversion of an entire channel list on the positive edge of the clock. In the second mode, the Data Acquisition Processor converts a single channel on the positive edge of the clock.

The input trigger and output trigger on all models also have two modes, a one-shot mode and a level triggered gate mode.

Software Triggers vs. Hardware Triggers for Input

DAPL provides a powerful software triggering mechanism which is suitable for most applications. For those applications that require precise synchronization to external hardware or that are too fast to take advantage of software triggering, hardware triggering is provided. Software triggering is more versatile than hardware triggering. In applications with sampling rates of less than 10 KHz, software triggering almost always provides a better solution than hardware triggering.

Software triggers rely on DAPL tasks to scan input data to detect events within the data. When an event is detected, a task asserts a software trigger. After the trigger is asserted, another task may act, based on the assertion. The most common action is to pass a number of values around the trigger event either to another task or to the PC. The trigger mechanism is much like the trigger on an oscilloscope. Since all of the processing functions of DAPL may be used to define events, however, much more complex events may be detected.

Hardware input triggers are implemented using a digital control line which is separate from the sampling stream. This control line starts and stops input sampling. Since the trigger line is not dependent on the input data, external hardware must be provided to detect events of interest.

Software triggers have several advantages over hardware triggers. First, a software trigger may be changed by changing a few lines in a DAPL command list. In contrast, a hardware trigger event must be detected by external hardware which may be inflexible and costly to modify. Second, software triggers scan input data to detect events, so pretrigger data are available. Because a hardware trigger starts the Data Acquisition Processor input section, no samples are taken before a trigger event. Finally, with software triggers DAPL provides precise timing information. With hardware triggers DAPL is not able to provide accurate timing information because hardware triggers start and stop input sampling at undefined times.

Hardware triggering does provide precise synchronization of acquisition to external events. Hardware triggering also allows detection of events which are too fast to process with software triggers.

Software and hardware triggering are implemented separately and may be used together.

External Input Clock

The external input clock is a positive-edge triggered TTL signal. The external input clock is activated by the command `CLOCK EXTERNAL` in an input procedure. The `TIME` command of an input procedure with input clocking enabled must be at least tSYNCH less than the period of the external clock. tSYNCH is defined at the end of this chapter.

External input clocking has two modes. The first mode, called Channel List Clocking, starts conversion of an entire channel list on the positive edge of the external clock. The second mode converts a single channel on the positive edge of the external clock. On the DAP 820 the selection between the modes is made by the position of a shunt on connector J16. As the Data Acquisition Processor is shipped from Microstar Laboratories, Channel List Clocking is selected. See for a diagram of J16.

Example:

```
IDEF A 5
   CLOCK EXTERNAL
   SET IPIPE0 S0
   SET IPIPE1 S1
   SET IPIPE2 S2
   SET IPIPE3 S3
   SET IPIPE4 S4
   TIME 1000
   . . . .
   END
```

In this application, external input clocking is enabled for the input procedure `A`. With Channel List Clocking selected, each positive edge of the external clock causes conversion of the entire channel list consisting of channel 0 (S0) to channel 4 (S4). The channels are converted in sequence with channel 0 synchronized to the positive edge of the external clock and each of the subsequent channels converted according to the `TIME` command. Channel 1 (S1) is converted 1000 µs following the edge of the external clock, channel 2 (S2) is converted 2000 µs following the edge of the external clock, up to channel 4 (S4) which is converted 4000 µs following the edge of the external clock. When using Channel List Clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command times the number of channels plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

In the previous application, the external clock must have a minimum period of 5000 µs plus tSYNCH. For example, on a DAP 820/103, the time for tSYNCH is 0.2 µs, so the minimum period of the external clock is 5000.2 µs. The value of tSYNCH is calculated as 4/n, where n is the CPU clock speed in MHz.

If single channel clocking is selected rather than Channel List Clocking, each positive edge of the external clock causes conversion of only one channel. The channels are converted in sequence. Each channel is synchronized to a positive edge of the external clock. In the previous application, channel 0 (S0) is converted on the first edge of the external clock, channel 1 (S1) is converted on the second edge of the external clock, and so on up to channel 4 (S4), which is converted on the fifth edge of the external clock. The channel list then is repeated with channel 0 converted again on the sixth positive edge of the external clock. When using single channel clocking, the period of the external clock (rising edge to rising edge) must be greater than the `TIME` command plus tSYNCH. The external clock may be as slow as required; there is no maximum period.

In the previous application, the external clock must have a period of 1000 µs plus tSYNCH. For example, on a DAP 820/103, the time for tSYNCH is 0.2 µs, so the minimum period of the external clock is 1000.2 µs.

Early External Input Clock Edges

To guarantee that the DAP 820 acquires only on external clock edges requires that there are no extra external input clock edges between 200 ns and tSYNCH plus the `TIME` command after the last acquisition. If this is not prevented, the Data Acquisition Processor will continue to operate, but the next acquisition will start according to the `TIME` command, not the external clock. Clocks earlier than 200 ns from the last acquisition are ignored.

In the previous example with channel list clocking, the external clock must not rise between 4000 µs plus 200 ns (4000.2 µs) and 5000 µs plus tSYNCH after the external clock that channel 0 converted upon. Extra clock edges less than 4000.2 µs after the clock for channel 0 are guaranteed to be ignored. Edges after that time and before 5000 µs plus tSYNCH can cause the next channel list to start 1000 µs after channel 4 (S4), instead of at the time of an external clock.

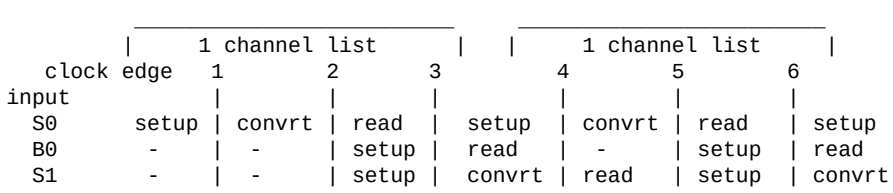
In the previous example with single channel clocking, the external clock should not rise between 200 ns and 1000 µs plus tSYNCH after any external clock that causes an acquisition. Any clock edge that does not meet this requirement will cause the next channel to be converted 1000 µs after the previous channel, instead of being converted upon an external clock edge.

Input Pipeline Timing

This section is of interest only when using external clocking or low latency with internal clocking.

Input sampling hardware has one pipeline stage for digital inputs and two pipeline stages for analog inputs. The number of pipeline stages and the type of the first input channel determines the number of clock pulses that are needed for the CPU to read a given value.

If the first channel is analog, analog conversion occurs on the first clock pulse and the value is read by the CPU on the second clock pulse. For channel list clocking, the last value in the channel list is read on the next external clock edge. The following timing diagram shows the relation of analog and digital samples when the first channel is analog. Note that for external clocking, one additional clock pulse is required before the first clock pulse shown in this diagram. See "Input Clocking Startup Considerations" later in this chapter for more details.



Note that `setup` indicates the setting up of analog or digital input circuits before the value is sampled, `convrt` indicates when the value is held and converted to digital, and `read` indicates when the value is read by the CPU. Each action occurs at or soon after the previous clock edge in the diagram.

If the first channel is a binary input and channel list clocking is used, the next clock pulse is not required to read the value from the last channel in the list. If one or more binary channels are used in a channel list with external clocking, it is best to make the first channel binary to simplify the timing. The following timing diagram shows relative timing when the first channel is binary.

```
          |     1 channel list      |    |     1 channel list     |
     clock edge 1         2        3         4        5        6
input           |         |        |         |        |        |
  B0      setup |  read   |  -     | setup   | read   |   -    | setup
  S0      setup |  convrt | read   | setup   | convrt | read   | setup
  S1       -    |  setup  | convrt | read    | setup  | convrt | read
```

The pipeline is important to consider in low latency applications. The time between the beginning of conversion and when the value is read by the CPU adds to the total response latency of the Data Acquisition Processor. For analog inputs one sample period is added to the latency. No significant latency is added for digital inputs.

External Output Clock

For most applications, there is no need to provide an output clock source to the Data Acquisition Processor; the on-board timer provides a wide range of update frequencies with fine time resolution. The main use of an output clock is to precisely match the output update rate to a standard frequency.

The external output clock on the Data Acquisition Processor is a positive-edge triggered TTL signal. Similar to the external input clock, the output clock is activated by the command `CLOCK EXTERNAL` in an output procedure. The `TIME` command of an output procedure with output clocking enabled must be at least tSYNCH shorter than the external clock period. tSYNCH and other times are defined at the end of this chapter. Unlike the external input clock, the first external output clock pulse is recognized.

On the DAP 820, all channels are updated simultaneously on the external clock.

Hardware Input Trigger

There are two modes for the input trigger. The first is a one-shot mode and the second is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an input procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an input procedure is started. Input sampling does not start until the trigger line is high. Sampling continues until a `STOP` command is issued or the number of samples specified by the `COUNT` command of the input procedure is reached. The first sampled value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the input procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external input trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, input sampling may start and stop repeatedly, depending on the level of the trigger signal. The input is sampled continuously when the trigger signal is high. Input sampling stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When input clocking is configured in Channel List Clocking mode, the input is stopped only at channel list boundaries. When input clocking is configured to clock single channels, the input is stopped on channel boundaries. The effect of this is that the start of sampling is precisely synchronized to the positive edge of the trigger signal, assuming that sampling has stopped. Sampling stops when the Data Acquisition Processor has completed sampling of either a channel list or a channel. When input sampling has been stopped with the gated trigger, synchronization of sampling to the positive edge of the trigger signal is the same as for the one-shot mode.

Hardware Output Trigger

There are two modes for the output trigger of a Data Acquisition Processors. The first mode is a one-shot mode and the second mode is a level-controlled gated mode. The mode of the hardware trigger is selected by a parameter to the `HTRIGGER` command in an output procedure. The three options for `HTRIGGER` are `ONESHOT`, `GATED`, and `OFF`. The default is `OFF`.

In the one-shot mode, the trigger line is held in a low state when an output procedure is started. Output updating does not start until the trigger line is high. Updating continues until a `STOP` command is issued or the number of updates specified by the `COUNT` command of the output procedure is reached. The first updated value is precisely synchronized to the trigger edge and all subsequent values are within ±tSYNCH of the `TIME` command of the output procedure. tSYNCH and other times are defined at the end of this chapter. The active period of the external output trigger must be greater than tTRIG_MIN to guarantee proper operation.

In the level-triggered gated mode, output updating may start and stop repeatedly, depending on the level of the trigger signal. The output is updated continuously when the trigger signal is high. Output updating stops when the trigger signal is low. The active period of the output trigger must be less than tTRIG_MAX to guarantee that only one update occurs.

When using the level-triggered gated mode without external output clocking, the hardware output trigger needs to be well-defined. Specifically, the high pulse width of the trigger cannot be in the range of *n * TIME +/- tSYNCH*, where n is any integer. A high pulse with such a width can cause data corruption and/or data being swapped between DACs.

When using the level-triggered gated mode with external output clocking, the hardware output trigger does not have to be well-defined.

On the DAP 820, all channels are updated simultaneously on the external clock.

Timing Considerations

When an external clock is used, the time of an event with respect to the start of sampling may only be determined if the period of the external clock is known. DAPL establishes event times as sample times. If the external clock period is variable or the period is unknown, the time of an event cannot be determined. The event's sample number may still be useful in other contexts. Note that the results of all frequency domain processing such as `FREQUENCY`, `FFT`, and `RFILTER` depend on the period of the external clock and may not be defined if the external clock period varies.

When hardware triggering is used, DAPL provides timing information relative to the start of each external trigger. In a case of a one-shot trigger, sampling or output updating starts on a single event so all timing information is relative to the trigger event. In the case of a gated trigger, sampling or output updating may start or stop at arbitrary times. Timing information may still be obtained if means are provided to distinguish one external trigger event from the next.

Input Clocking Startup Considerations

For the DAP 820, following the start of an input procedure with external input clocking enabled, there is a delay of one external clock edge before the first input sample is taken. This delay is required to allow clean synchronization of the internal clock to the external input clock. This means that the first positive edge of the external input clock, following the `START` command to the input procedure, is ignored. The second positive edge of the external input clock may be as close as 50 ns to the first positive edge.

If loss of the first external clock edge is unacceptable, the input trigger, configured in the level triggered gated mode, may be used as an input clock. This requires the input trigger to have a short active period. The active period of the input trigger should be more than tTRIG_MIN; this allows for any speed of acquisition. The active period of the input trigger must be less than tTRIG_MAX to guarantee that only one acquisition occurs.

If the input trigger is held inactive until the input procedure is started, the first positive edge of the input trigger will cause a conversion. Note that this approach to clocking seldom makes sense when the external clock source is free running; in most cases, using external hardware to provide a clean trigger signal will lose one clock edge.

Using the Input Trigger with External Input Clocking

Input triggering may be used with external input clocking. When these functions are used together, however, precise synchronization of acquisition to a trigger edge is not available. The reason for the loss of synchronization is that the Data Acquisition Processor has no control over the external clock.

For the DAP 820, the time from a trigger edge until the first conversion will be from 1 to 2 external clock cycles, assuming input sampling has stopped. To guarantee recognition of an external trigger after 1 external clock cycle, the external trigger must meet a setup time of tTCSETUP to the positive edge of the external clock. Each time a trigger is reasserted there is a 1 to 2 clock delay before acquisition starts. When a hardware trigger is used with the internal clock, the Data Acquisition Processor synchronizes its clock to the edge of the external trigger so there is no synchronization condition.

Using the Output Trigger with External Output Clocking

Output triggering may be used with external output clocking. Unlike input clocking, updates can occur on the first external clock after the trigger is asserted. To guarantee recognition of an external clock, the external trigger must meet a setup time of tTCSETUP to the positive edge of the external clock.

Timing tables

tSYNCH	four CPU clock cycles	Time needed to synchronize an internal clock to an external clock
tTRIG_MIN	60 ns	Minimum high period for the input and output trigger
tEXTCLK_PW	25 ns	Minimum high or low period of an external clock
tTCSETUP	50 ns	External trigger to external clock setup time
tITRIG_MAX	200 ns	Maximum high period of the input trigger to guarantee a single conversion
tINSKEW	200 ns	Time from input clock or trigger to conversion value held
tOUTSKEW	30 ns	Time from output clock until start of DAC slewing

7. MSTB 010 DAP 820, DAP 820, DAP 820 Termination Board

The Microstar Laboratories Input/Output Termination Board, part number MSTB 010, is a 64-point quick-connect termination board for all connections on the DAP 820 input/output connector. The Input/Output Termination Board provides a ground connection for each input signal and each output signal, allowing easy connection to discrete devices.

All input connections are labeled with both the signal name and the pin number of the 50-pin connector on the Data Acquisition Processor. The pin numbers are discussed in Chapter 4.

Note: The Input/Output Termination Board should not be connected or disconnected while the Data Acquisition Processor is powered.

Analog Inputs

The analog inputs of the Input/Output Termination Board come from the factory configured for voltage input. The inputs can be configured for current input or for input voltages that exceed Data Acquisition Processor specifications.

The Input/Output Termination Board also can be used for differential analog inputs. A differential input is used to measure the difference between two voltages. The negative terminal voltage is subtracted from the positive terminal voltage. When a differential voltage is measured, a ground sense line must be connected between the Input/Output Termination Board and the signal source. Table 1 shows the correspondence between differential and single-ended inputs.

Table 1.

Single-Ended Input	Differential Input
S0	D0-
S1	D0+
S2	D1-
S3	D1+
S4	D2-
S5	D2+
S6	D3-
S7	D3+

Analog Outputs

The DAP 820 digital-to-analog converter outputs are available on the Input/Output Termination Board, along with a ground return for each output. The output current from each digital-to-analog converter output is rated at ± 5 milliamps, but it is recommended that this current not exceed ± 1 milliamp. The digital-to-analog converter outputs are voltage outputs.

Digital Input/Output

All digital input connections are labeled DIx where x is the input number; x ranges from 0 to 7. Each input connection has an adjacent ground connection. The inputs are FCT TTL; they sink no more than 20 microamps for a “1” input and source no more than 0.7 milliamps for a “0” input. An input voltage greater than 2V is interpreted as a “1” and an input voltage less than 0.8V is interpreted as a “0”.

Digital input pins may have signals applied when the Data Acquisition Processor is off.

Note: If a voltage greater than 5V or less than 0V is applied to an input, damage to the Data Acquisition Processor may occur.

All digital output connections on the Digital Termination Board are labeled DOx, where x is the output number; x ranges from 0 to 7. Each output has an adjacent ground connection. The outputs are FCT TTL; they can sink no more than 12 milliamps for a “0” output and can source no more than 15 milliamps for a “1” output. The output voltage for a “1” is at least 2.4V and the output voltage for a “0” is less than 0.5V.

All digital ground connections are electrically connected on the Input/Output Termination Board, and are connected to the Data Acquisition Processor ground. All digital signals connected to an Input/Output Termination Board must share the PC’s ground as a common reference.

Note: If the digital output current is extended beyond maximum ratings, damage to the Data Acquisition Processor is possible.

Control Lines

The Input/Output Termination Board has connections to DAP 820 clock and trigger lines. The connection labeled `XC0` is the external input clock input. The buffered internal input clock output is labeled `INC`. The connection labeled `XC1` is the external output clock input. The external trigger input connection is labeled `TRIG`.

Power Supplies

The Data Acquisition Processor has unregulated ± 18 volt supply voltages; these are available on the Input/Output Termination Board. The maximum allowable current drain from these supplies is 20 milliamps per side. If more current than this is required, an external power supply should be used instead of the Data Acquisition Processor's ± 18 volt supply. The Input/Output Termination Board also has connections for the Data Acquisition Processor +5V power supply. The 5V supply has two connections on the Input/Output Termination Board; the output current is rated at 500 milliamps per connection.

Hardware Configuration

The Input/Output Termination Board is connected to a DAP 820 using a 50-line ribbon cable, part number MSCBL 050-01, or a 50-line round shielded cable, part number MSCBL 048-01. MSCBL 050-01 or MSCBL 048-01 connects the input/output connector of a DAP 820 to connector J1 of the Input/Output Termination Board.

Current Input

To configure a current input, place a resistor in the location on the termination board corresponding to the input pin being reconfigured. Figure 5 and Table 2 show resistor placement. The appropriate size for this resistor can be calculated using Ohms law, given the maximum input current and the input voltage range of the Data Acquisition Processor.

```
Ohm's Law: Resistance = Voltage / Current
```

The Data Acquisition Processor is shipped from the factory with an input range of +/- 5 volts. The accuracy of the measurements made in this configuration depends on the precision of the resistors used and this should be taken into consideration when selecting the resistors. Microstar Laboratories recommends using resistors with a 1% or better tolerance.

Excess power dissipated in the resistor causes heating; this changes the resistance value, decreasing the accuracy of the measurements. The recommended maximum power dissipation is 0.1 watt.

```
Power Calculation: Power = current^2 * resistance
```

For current input, a current source is connected to the `Sx` terminal and the ground return is connected to the `Gx` terminal. To convert voltage input `S0` into a current input that generates 1 to 5 volts with an input current of 4 to 20 milliamps, a 250 ohm resistor is inserted in the `R2` location. In this case, the maximum power dissipated in the resistor is 0.1 watt at +5 volts; this is the maximum recommended power dissipation. Figure 3 illustrates the connections for this example.

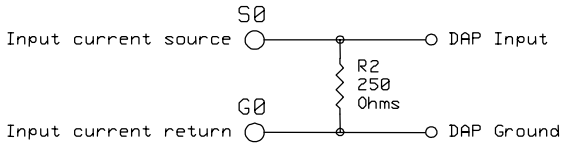


Figure 3.

Voltage Divider

The termination board can be configured for applications requiring input voltages greater than that allowed by the Data Acquisition Processor. This is accomplished by soldering a resistive voltage divider in the location provided on the termination board. Before this can be done, a trace on the termination board must be cut. Above each odd numbered resistor there is a row of five small holes. Between two of the holes there is a white "X". The trace at the X must be cut.

Once this trace is cut, the resistors for the voltage divider are soldered into place. The resistor on the ground side of the divider is placed in an even numbered resistor location and the resistor on the input signal side of the divider is placed in an odd numbered resistor location. Figure 5 and Table 2 illustrate resistor placement for each input.

After both resistors are soldered into place, signals may be connected between the `Sx` and `Gx` terminals. Test the voltage divider circuit before connecting the circuit to the Data Acquisition Processor.

Note: Be careful to avoid applying an input voltage that exceeds Data Acquisition Processor specifications.

Warning: If the trace on the termination board is not cut, the high voltage input is connected directly to the Data Acquisition Processor input; this may damage or even destroy the Data Acquisition Processor.

For example, to configure input `S0` so that an input range of 0 to 20 volts is scaled down to a range of 0 to 5 volts, a resistor ratio of 3:1 is needed.

Voltage Divider Equation: $V_{out} = V_{in} * R1/(R1+R2)$

Resistance values of 1500 and 500 ohms may be used. The trace beneath the X above `R1` is cut. Then the 500 ohm resistor is placed in the `R2` position and the 1500 ohm resistor is placed in the `R1` position. Since 500 ohm resistors are not commonly available, a 510 ohm resistor would typically be used instead, resulting in a small error in the division ratio. This error is linear and can be corrected by multiplying by a constant in DAPL. Figure 4 illustrates the circuit for this example.

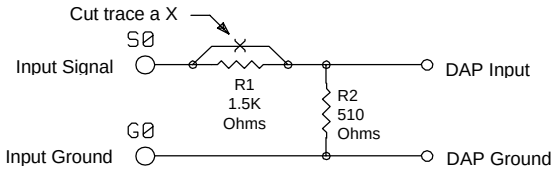


Figure 4.

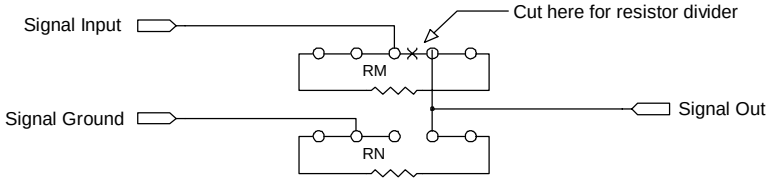


Figure 5.

Note: To avoid exceeding Data Acquisition Processor input voltage specifications, make sure both resistors are securely soldered in the correct locations and the trace beneath the X is completely cut before using the circuit.

Table 2.

Terminal	Current Input Resistor *	Voltage Divider Resistors
S0, G0	R2	R2, R1
S1, G1	R4	R4, R3
S2, G2	R6	R6, R5
S3, G3	R8	R8, R7
S4, G4	R10	R10, R9
S5, G5	R12	R12, R11
S6, G6	R14	R14, R13
S7, G7	R16	R16, R15

* The current input resistor is placed in the RN location shown in the previous figure.

** The first resistor is on the ground side of the voltage divider (RN), the second is on the input signal side (RM), as shown in the previous diagram. For example, R2 is RN and R1 is RM. Figure 5 shows the resistor placement.

Table 2 and Figure 5 can be used to locate the appropriate resistors when using either the current input or voltage division configuration. Figure 5 shows schematically how the inputs and grounds on the termination board are connected.

Cold Junction Reference

The Input/Output Termination Board is available with a cold junction reference circuit option. This circuit is used to measure the temperature of the “cold junction” at the termination board. Since the cold junction temperature is the same for all thermocouples connected to a termination board, only one cold junction reference circuit is needed for any number of thermocouples.

The cold junction reference circuit generates a voltage which is temperature dependent. When jumper J5 is installed the output of this circuit are connected to single-ended input S7 of the termination board. The Data Acquisition Processor samples this voltage and the resultant information is used in the `THERMO` command for cold junction compensation. When the cold junction reference circuit and jumper J5 are installed, no other inputs should be connected to the S7 terminal, as it is connected to the cold junction reference circuit. Removing jumper J5 will disconnect the cold junction reference circuit from the S7 terminal.

The cold junction reference circuit is implemented with a Linear Technology LT1025 integrated circuit. This part provides a 10 mV/°C voltage output. The output voltage can be modeled by the following formula.

$$V_o = 10mV/°C(T) + (10mV/°C)(5.5x10E\text{-}4)(T\text{-}25°C)^2$$

The LT1025 has a nearly linear voltage output. For temperatures near room temperature, the quadratic error term is negligible and the voltage output is:

$$V_o = 10mv/°C * T$$

See the Applications Manual for an example using the cold junction reference circuit.

MSXB 019 DAP 820 Analog Expansion Board

The Microstar Laboratories Analog Input Expansion Termination Board, part number MSXB 019, multiplexes 32 analog inputs into a DAP 820. One Analog Input Expansion Termination Board can be connected to a Data Acquisition Processor, providing up to 32 analog inputs.

The MSXB 019 features fault-protected inputs and socketed multiplexer chips.

Note: MSXB 019 uses different cabling than other DAP 820 expansion boards; it is available primarily for compatibility with existing systems. For new systems, MSXB 024 may provide a better solution.

Hardware Configuration

An Analog Input Expansion Board is connected to a Data Acquisition Processor using cable part number MSCBL 047-01. MSCBL 047-01 is a 50-line ribbon cable which connects the analog I/O connector of the Data Acquisition Processor to connector `J1` of the Analog Input Expansion Board.

Note: The Analog Input Expansion Board should not be connected to or disconnected from a Data Acquisition Processor while the Data Acquisition Processor is powered.

Connectors `J2`, `J3`, `J4`, and `J5` of the Analog Input Expansion Board accept 32 single-ended or 16 differential analog input signals. These 50-pin connectors have the same pinout as the DAP 820 analog I/O connector, with ground lines adjacent to the signal lines. Signals may be connected to an Analog Input Expansion Board using Analog Termination Boards, part number MSTB 010-01, 50 wire cable kits, part number MSCBL 032-01K, or 50 wire IDC cable kits, part number MSCBL 031-01K.

Note: The inputs pins of the Analog Input Expansion Board are ordered differently than the input pins specified in DAPL `SET` commands. Use the following tables to map the DAPL input pins to the corresponding Analog Input Expansion Board input pins. DAPL 4.3 users: see the next section, “Mapping Input Pins Using DAPL 4.3.”

Single-Ended Inputs

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
S0	J5	36	S0
S1	J5	35	S1
S2	J4	36	S0
S3	J4	35	S1
S4	J3	36	S0
S5	J3	35	S1
S6	J2	36	S0
S7	J2	35	S1
S8	J5	34	S2
S9	J5	33	S3
S10	J4	34	S2
S11	J4	33	S3
S12	J3	34	S2
S13	J3	33	S3
S14	J2	34	S2
S15	J2	33	S3
S16	J5	32	S4
S17	J5	31	S5
S18	J4	32	S4
S19	J4	31	S5
S20	J3	32	S4
S21	J3	31	S5
S22	J2	32	S4
S23	J2	31	S5
S24	J5	30	S6
S25	J5	29	S7
S26	J4	30	S6
S27	J4	29	S7
S28	J3	30	S6
S29	J3	29	S7
S30	J2	30	S6
S31	J2	29	S7

Differential Inputs

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
D0	J5	36, 35	D0
D1	J4	36, 35	D0
D2	J3	36, 35	D0
D3	J2	36, 35	D0
D4	J5	34, 33	D1
D5	J4	34, 33	D1
D6	J3	34, 33	D1
D7	J2	34, 33	D1
D8	J5	32, 31	D2
D9	J4	32, 31	D2
D10	J3	32, 31	D2
D11	J2	32, 31	D2
D12	J5	30, 29	D3
D13	J4	30, 29	D3
D14	J3	30, 29	D3
D15	J2	30, 29	D3

Mapping Input Pins Using DAPL 4.3

DAPL 4.3 provides an option that maps the pins of an Analog Input Expansion Board so they match the order on the Data Acquisition Processor analog connector. Use the DAPL command `OPTION AINEXPAND=ON` to set DAPL so that it automatically maps the Analog Input Expansion Board input pins to the input pins of the `SET` command. When `AINEXPAND` is on, the `SET` command maps to the Analog Input Expansion Board as shown in the following table:

DAPL Input Pins	Analog Input Expansion Board Pins
S0 ... S7	J5: S0 ... S7
S8 ... S15	J4: S0 ... S7
S16 ... S23	J3: S0 ... S7
S24 ... S31	J2: S0 ... S7
D0 ... D3	J5: D0 ... D3
D4 ... D7	J4: D0 ... D3
D8 ... D11	J3: D0 ... D3
D12 ... D15	J2: D0 ... D3

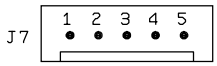
Software Configuration

DAPL automatically generates expansion control signals, as specified by input procedure `SET` commands. For example, the following input procedure reads from expanded analog inputs:

```
RESET
IDEF A 5
  SET IPIPE0 S0
  SET IPIPE1 S27
  SET IPIPE2 D3
  SET IPIPE3 D4
  SET IPIPE4 D8 100
  TIME 10000
  END
PDEF B
  PRINT
  END
START A, B
```

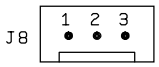
External Clock and Trigger Connection

An external input clock and trigger signal can be connected to connector J7 of the Analog Input Expansion Board to provide external hardware clocking and triggering for inputs. See the connector chapters and Chapter 6 for more information about hardware triggering. In addition to the clock and trigger inputs, the on-board input clock is available as an output on J7. The pinout of connector J7 is:



Pin 1 of connector J7 is closest to the connector marked J9. Pin 1 is digital ground and pin 5 is the digital +5 Volt supply. Pin 2 is connected to the Data Acquisition Processors hardware trigger input. Pin 3 is connected to the Data Acquisition Processors internal acquisition clock output. Pin 4 is connected to the Data Acquisition Processors external acquisition clock input. External signals connected to J7 must be in the standard TTL range of 0 to +5 volts. The pins on J7 connect directly to the pins on the analog I/O connector of the Data Acquisition Processor.

An external output clock signal can be connected to connector J8 of the Analog Input Expansion Board to provide external hardware clocking for outputs. See the connector chapters and Chapter 6 for more information about external clocking. The pinout of connector J8 is:



Pin 1 of connector J8 is closest to the connector marked J7. Pin 1 is digital ground and pin 3 is the digital +5 Volt supply. Pin 2 is connected to the Data Acquisition Processors external output clock input. External signals connected to J8 must be in the standard TTL range of 0 to +5 volts. The pins on J8 connect directly to the pins on the analog I/O connector of the Data Acquisition Processor.

MSXB 024 DAP 820 Termination Expansion

The Microstar Laboratories Analog Input Expansion Termination Board, part number MSXB 024, multiplexes 32 analog inputs into a DAP 820. One Analog Input Expansion Termination Board can be connected to a Data Acquisition Processor, providing up to 32 analog inputs.

The MSXB 024 does not provide access to the digital inputs or digital outputs. Digital signals can be accessed by means of a daisy-chained MSTB 010 termination board.

MSXB 024 features fault-protected inputs and socketed multiplexer chips.

Hardware Configuration

An Analog Input Expansion Termination Board is connected to a Data Acquisition Processor using cable part number MSCBL 050-01 or MSCBL 048-01. MSCBL 050-01 is a 50-line ribbon cable that connects the analog I/O connector of the Data Acquisition Processor to connector J1 of the Analog Input Expansion Termination Board. MSCBL 048-01 is a 50-line round shielded cable that connects the analog I/O connector of the Data Acquisition Processor to connector J1 of the Analog Input Expansion Termination Board.

Note: The Analog Input Expansion Termination Board should not be connected to or disconnected from a Data Acquisition Processor while the Data Acquisition Processor is powered.

Connectors `J2`, `J3`, `J4`, and `J5` of the Analog Input Expansion Termination Board accept terminations for 32 single-ended or 16 differential analog input signals and their corresponding ground lines.

The analog inputs on `J2`, `J3`, `J4`, and `J5` are labeled according to the DAPL 4.3 convention with the AINEXPAND option set to ON. Use the DAPL command `OPTION AINEXPAND=ON`.

`J6` provides terminations for the DAC analog outputs and their corresponding ground return lines.

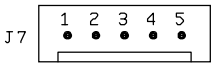
Software Configuration

DAPL automatically generates expansion control signals, as specified by input procedure `SET` commands. For example, the following input procedure reads from expanded analog inputs:

```
RESET
IDEF A 5
  SET IPIPE0 S0
  SET IPIPE1 S27
  SET IPIPE2 D3
  SET IPIPE3 D4
  SET IPIPE4 D8 100
  TIME 10000
  END
PDEF B
  PRINT
  END
START A, B
```

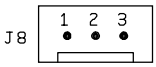
External Clock and Trigger Connection

An external input clock and trigger signal can be connected to connector J7 of the Analog Input Expansion Termination Board to provide external hardware clocking and triggering for inputs. See the connector chapters and Chapter 6 for more information about hardware triggering. In addition to the clock and trigger inputs, the on-board input clock is available as an output on J7. The pinout of connector J7 is:



Pin 1 of connector J7 is closest to the connector marked J1. Pin 1 is digital ground and pin 5 is the digital +5 Volt supply. Pin 2 is connected to the Data Acquisition Processors hardware trigger input. Pin 3 is connected to the Data Acquisition Processors internal acquisition clock output. Pin 4 is connected to the Data Acquisition Processors external acquisition clock input. External signals connected to J7 must be in the standard TTL range of 0 to +5 volts. The pins on J7 connect directly to the pins on the analog I/O connector of the Data Acquisition Processor.

An external output clock signal can be connected to connector J8 of the Analog Input Expansion Termination Board to provide external hardware clocking for outputs. See the connector chapters and Chapter 6 for more information about external clocking. The pinout of connector J8 is:



Pin 1 of connector J8 is closest to the connector marked J7. Pin 1 is digital ground and pin 3 is the digital +5 Volt supply. Pin 2 is connected to the Data Acquisition Processors external output clock input. External signals connected to J8 must be in the standard TTL range of 0 to +5 volts. The pins on J8 connect directly to the pins on the analog I/O connector of the Data Acquisition Processor.

Cold Junction Reference

The analog termination board has a cold junction temperature reference circuit. This circuit is used to measure the temperature of the “cold junction” at the termination board when using thermocouples. Since the cold junction temperature is the same for all thermocouples connected to a termination board, only one cold junction reference circuit is needed for any number of thermocouples.

The cold junction reference circuit generates a voltage that is temperature dependent. The output of this circuit is connected to input S8 of the termination board. The Data Acquisition Processor samples this voltage and the resultant information is used in the `THERMO` command for cold junction compensation.

To use the cold junction reference circuit, both shunts must be installed on `J10`.

Note: When the cold junction reference circuit is used no other inputs may be connected to the S31 terminal, because it is connected to the cold junction reference circuit.

The cold junction reference circuit consists of a Linear Technology LT1025A integrated circuit. The LT1025A has a linear voltage output which is directly proportional to the temperature in degrees Celsius. The LT1025A outputs 0 Volts at 0° Celsius and 10 millivolts for every degree above zero. At 25° Celsius, the LT1025A will output 250 millivolts. The cold junction reference circuit will not operate at temperatures below 0° Celsius and may not function properly at temperatures above 50° Celsius.

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