

MSXB 018 Accessory Board Manual

Analog Input Expansion Board

Version 1.40

Microstar Laboratories, Inc.

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Part Number MSXB018M140

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MSXB 018: Analog Input Expansion

The Microstar Laboratories Analog Input Expansion Board, part number MSXB 018, multiplexes 64 analog inputs into a Data Acquisition Processor. Up to eight Analog Input Expansion Boards can be connected to a Data Acquisition Processor, providing 512 analog inputs.

The MSXB 018 Analog Input Expansion Board features high-speed, fault-protected inputs and socketed multiplexer chips.

Hardware Configuration

An Analog Input Expansion Board is connected to a Data Acquisition Processor using either cable MSCBL 040-01 or cable MSCBL 041-01.

- MSCBL 040-01 is a 68-line round shielded cable, which can be used with EMC-compliant systems.
- MSCBL 041-01 is a 68-line flat ribbon cable, which cannot be used with EMC-compliant systems.

Either cable connects the analog I/O connector of the Data Acquisition Processor to connector J1 of the Analog Input Expansion Board.

Warning: The Analog Input Expansion Board should not be connected to or disconnected from a Data Acquisition Processor while the Data Acquisition Processor is powered.

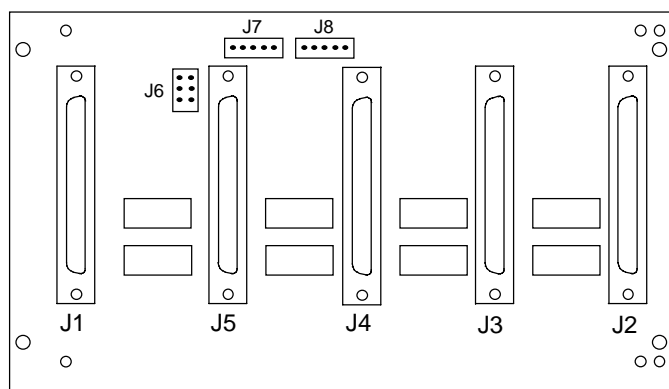


Figure 1. MSXB 018 Connector Locations

Connectors J2, J3, J4, and J5 of the Analog Input Expansion Board accept 64 single-ended or 32 differential analog input signals. These 68-pin connectors have the same pinout as the Data Acquisition Processor analog I/O connector, with ground lines adjacent to the signal lines. Signals may be connected to an Analog Input Expansion Board using Analog Termination Boards, part number MSTB 009.

Note: The input pin order on the J2-J5 connectors does not match the S0-S15 DAPL input pin order. The following tables show how the Analog Input Expansion Board input signals map to DAPL input

pins. For information about pin mapping options, see the section, “Mapping Input Pins.”

Table 1. Single-Ended Input Pin Mapping

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
S0	J5	53	S0
S1	J5	52	S1
S2	J5	45	S8
S3	J5	44	S9
S4	J4	53	S0
S5	J4	52	S1
S6	J4	45	S8
S7	J4	44	S9
S8	J3	53	S0
S9	J3	52	S1
S10	J3	45	S8
S11	J3	44	S9
S12	J2	53	S0
S13	J2	52	S1
S14	J2	45	S8
S15	J2	44	S9
S16	J5	51	S2
S17	J5	50	S3
S18	J5	43	S10
S19	J5	42	S11
S20	J4	51	S2
S21	J4	50	S3
S22	J4	43	S10
S23	J4	42	S11
S24	J3	51	S2
S25	J3	50	S3
S26	J3	43	S10
S27	J3	42	S11
S28	J2	51	S2
S29	J2	50	S3
S30	J2	43	S10
S31	J2	42	S11

Table 1. Single-Ended Input Pin Mapping, continued

Corresponding

DAPL Input Pin	Connector	Connector Pin	Termination Board Label
S32	J5	49	S4
S33	J5	48	S5
S34	J5	41	S12
S35	J5	40	S13
S36	J4	49	S4
S37	J4	48	S5
S38	J4	41	S12
S39	J4	40	S13
S40	J3	49	S4
S41	J3	48	S5
S42	J3	41	S12
S43	J3	40	S13
S44	J2	49	S4
S45	J2	48	S5
S46	J2	41	S12
S47	J2	40	S13
S48	J5	47	S6
S49	J5	46	S7
S50	J5	39	S14
S51	J5	38	S15
S52	J4	47	S6
S53	J4	46	S7
S54	J4	39	S14
S55	J4	38	S15
S56	J3	47	S6
S57	J3	46	S7
S58	J3	39	S14
S59	J3	38	S15
S60	J2	47	S6
S61	J2	46	S7
S62	J2	39	S14
S63	J2	38	S15

Table 2. Differential Input Pin Mapping

DAPL Input Pin	Connector	Connector Pin	Corresponding Termination Board Label
D0	J5	53, 52	D0
D1	J5	45, 44	D4
D2	J4	53, 52	D0
D3	J4	45, 44	D4

D4	J3	53, 52	D0
D5	J3	45, 44	D4
D6	J2	53, 52	D0
D7	J2	45, 44	D4
D8	J5	51, 50	D1
D9	J5	43, 42	D5
D10	J4	51, 50	D1
D11	J4	43, 42	D5
D12	J3	51, 50	D1
D13	J3	43, 42	D5
D14	J2	51, 50	D1
D15	J2	43, 42	D5
D16	J5	49, 48	D2
D17	J5	41, 40	D6
D18	J4	49, 48	D2
D19	J4	41, 40	D6
D20	J3	49, 48	D2
D21	J3	41, 40	D6
D22	J2	49, 48	D2
D23	J2	41, 40	D6
D24	J5	47, 46	D3
D25	J5	39, 38	D7
D26	J4	47, 46	D3
D27	J4	39, 38	D7
D28	J3	47, 46	D3
D29	J3	39, 38	D7
D30	J2	47, 46	D3
D31	J2	39, 38	D7

Mapping Input Pins

DAPL (versions 4.3 and later) and DAPL 2000 provide a DAPL OPTION that maps the pins of an Analog Input Expansion Board to the DAPL input pin order.

When OPTION AINEXPAND = ON, the SET command maps to the Analog Input Expansion Board as shown in the following table:

Table 3. AINEXPAND Pin Mapping

DAPL Input Pins	Analog Input Expansion Board Pins
S0 ... S15	J5: S0 ... S15
S16 ... S31	J4: S0 ... S15
S32 ... S47	J3: S0 ... S15
S48 ... S63	J2: S0 ... S15
D0 ... D7	J5: D0 ... D7
D8 ... D15	J4: D0 ... D7
D16 ... D23	J3: D0 ... D7
D24 ... D31	J2: D0 ... D7

The diagram below shows the signal connections for one Analog Input Expansion Board with AINEXPAND=ON:

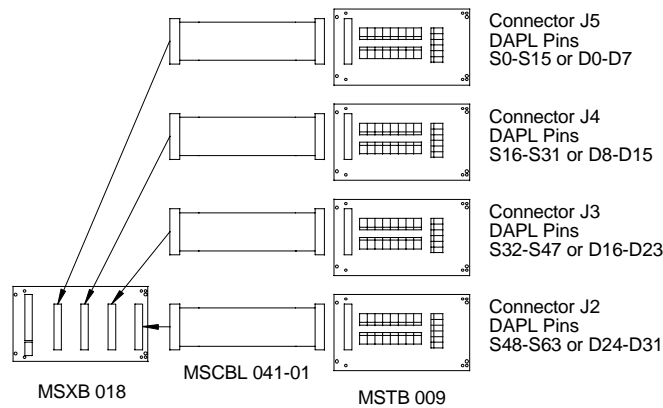


Figure 2. AINEXPAND Mapping for One Expansion Board

Each termination board is labeled S0-S15. The inputs on each termination board map sequentially to the DAPL input pins. For example, the termination board connected to J3 has termination input S0 mapping to DAPL pin S32, S1 mapping to S33, S2 mapping to S34, etc.

Input Range Selection

Each Analog Input Expansion Board must be configured to recognize a specific input pin range. Connector J6 selects this range.

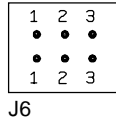


Figure 3. Input Range Selection Header

The bottom of connector J6 is closest to connector J5. The input pin range is selected by adding an offset according to the following table:

Table 4. Input Range Configuration

Single-Ended Input Range	Differential Input Range	Board Number	Jumpers
0 - 63	0 - 31	0	1, 2, 3
64 - 127	32 - 63	1	1, 2
128 - 191	64 - 95	2	1, 3
192 - 255	96 - 127	3	1
256 - 319	128 - 159	4	2, 3
320 - 383	160 - 191	5	2
384 - 447	192 - 223	6	3
448 - 511	224 - 255	7	none

External Clocking and Triggering Connections

External clocking and triggering signals can be connected to the Analog Input Expansion Board to provide hardware triggering and clocking. See the Data Acquisition Processor manual for more information about hardware clocking and triggering.

Input clocking and triggering signals can be connected to J7. The top of connector J7 is closest to the edge of the board. The pin numbering for connector J7 is given in the following table:

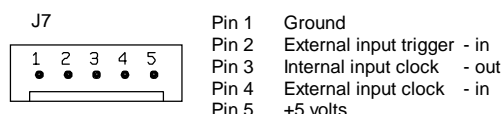


Figure 4. Input Clocking and Triggering Header

Output clocking and triggering signals can be connected to J8. The top of connector J8 is closest to the edge of the board. The pin numbering for connector J8 is given in the following table:

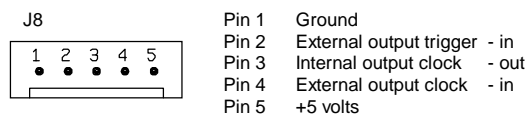


Figure 5. Output Clocking and Triggering Header

External signals connected to J7 and J8 must be in the standard TTL range of 0 to +5 volts. The pins on J7 and J8 connect directly to the pins on a Data Acquisition Processor.

Sampling Speed with External Expansion

When using external expansion with fault-protected inputs, the multiplexer settling time must be added to the settling time of the on-board analog circuits. This is restrictive only at high sampling speeds. For fault-protected multiplexers, add 2 μ s to the minimum sample rate of the Data Acquisition Processor.

Software Configuration

DAPL automatically generates expansion control signals, as specified by input procedure `SET` commands. For example, the following input procedure reads from expanded analog inputs:

```
RESET
  IDEF A 5
  SET IPIPE0 S0
  SET IPIPE1 S57
  SET IPIPE2 D23
  SET IPIPE3 D4
  SET IPIPE4 D18 100
  TIME 10000
END
PDEF B
  PRINT
  END
START A, B
```