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Technical Note TN-106 **Version 1.0**

Technical Product Information for the DAP 3400a™

The Data Acquisition Processor™ from Microstar Laboratories is a complete data acquisition system that occupies one expansion slot in a PC. Data Acquisition Processors are suitable for a wide range of applications in laboratory and industrial data acquisition and control.

The DAP 3400a is high-performance Data Acquisition Processor specialized for fast analog sampling.

Features of the DAP 3400a model:

- Intel i486DX4 processor onboard
- 8M of DRAM onboard memory
- Compatible with other a-Series boards
- Complies with the European EMC directive and is CE marked
- Works with the AT ISA bus for 286/386/486/Pentium PC platforms
- Transfers data to the PC at high rates — up to 816K samples per second
- Allows fast real-time processing
- Sampling period resolution of 50 ns
- Onboard DSP routines
- Four separate analog to digital converters
- Samples analog inputs at up to 800K samples per second on each of four converters
- Aggregate sample rate of 3.2M samples per second
- Inherent simultaneous sampling
- Expandable analog inputs
- No analog outputs
- No digital I/O

There is one DAP 3400a model: the DAP 3400a/445. This technical note describes the DAP 3400a in terms of its similarities with other Data Acquisition Processor boards, software speed and functionality, and hardware characteristics.

The DAP 3400a is the highest-performance Data Aquisition Processor produced by Microstar Laboratories. The DAP 3400a is well suited for applications that require high aggregate analog sample rates or high-speed simultaneous sampling. In order to make room for the extra analog input hardware, the analog outputs and digital I/O were removed. If analog outputs or digital I/O is needed, the DAP 3400a may be used with a DAP 3200e™/415 or other Data Acquisition Processor. A typical system may consist of several DAP 3400a/445 boards and one or more DAP 3200e/415 boards. The DAP 3200e/415 inputs may be synchronized with the inputs of the DAP 3400a/445.

The DAP 3400a is compatible with the DAP 3200e boards, with the exception of the analog I/O connector. The DAP 3400a uses a 68-pin analog connector, which is compatible with the DAP 1216e™, DAP 2416e™, and a-Series Data Acquisition Processors. All configurations use the same termination and expansion boards whether the Data Acquisition Processor is a DAP 1216e,

DAP 2416e, or a-Series. Since the DAP 3400a has no digital I/O, the only relevant termination and expansion boards are for analog input.

Like every a-Series and e-Series Data Acquisition Processor, the DAP 3400a is compatible with the AT ISA bus for 286/386/486/Pentium industry standard platforms. Dual 1K word BiFIFO buffers allow fast data transfer to and from the host PC.

The main differences between the DAP 3400a/445 and DAP 3200e™/415 is that the DAP 3400a has four analog to digital converters, no analog outputs, no digital I/O, and no programmable gain amplifier. The DAP 3400a has twice the memory of the DAP 3200e/415 and more than four times the aggregate analog sample rate along with built-in simultaneous sampling. The DAP 3400a and DAP 3200e may be used together to make a system with inputs as well as outputs and digital I/O.

The DAP 3400a uses DAPL 2000™, a 32-bit version of DAPL™, the onboard multitasking operating system. DAPL is a complete software environment for real-time data acquisition. Tasks that perform averaging, triggering, PID control, fast Fourier transforms, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data aquisition application. Custom commands can be written with the Developer's Toolkit for DAPL™ if multiple commands need to be combined, or if a specific application cannot be implemented with standard DAPL commands. Table 1 shows some standard DAPL commands tabulated with a comparision of their speed of execution on the DAP 3400a and DAP 2400e™/6, which has an onboard DSP processor.

Table 1: Comparison of DAPL command speeds —DAP 2400e/6 and DAP 3400a/445

DAPL Command	Description	Time of Execution[i] on DAP 3400a/445	Time of Execution[1] on DAP 2400e/6
`AVERAGE`	Averages groups of 120 data points	0.64 µs	3.4 µs
`FFT`	FFT of blocksize of 1024 points, amplitude spectrum	3.23 ms	12.4 ms
DAPL Expression: `P3 = P1 * P2`	Arithmetic operation, scales input magnitude	1.94 µs	54 µs
`LIMIT/WAIT`	Generates/processes level-based triggers	0.71 µs	3.8µs
`INTERP`	Interpolates 2 vectors	1.76 µs	55.9 µs

The DAP 3400a is an excellent choice for applications where there is a need for a large amount of real-time processing of data, for applications requiring fast sample rates, and for applications requring high speed simultaneous sampling. The DAP 3400a/445 features a clock-tripled Intel DX4 processor that executes three internal clock cycles for each external clock cycle, with an internal clock rate of 96 MHz. The Intel DX4 processor features a hardware multiplier and a large internal cache, making it particularly well suited for DSP operations.

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[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation. Kernel speeds for the task are smaller.

Times for the DAP 3400a were found by sampling four channels simultaneously, then dividing by four to get a per-channel sample rate.

From the point of view of DSP-intensive applications, the main difference between the DAP 3400a and the DAP 2400e is that, while the DAP 3400a has a 486 processor, the DAP 2400e has a 80C186 processor and a DSP coprocessor. The DAP 3400a handles DSP routines in the DX4 processor. While it may seem that a dedicated DSP coprocessor would process DSP routines faster than a 486, the DAP 3400a is faster than the DSP coprocessor in all cases, often by a large margin. For non-DSP commands, the DAP 3400a is much faster than the DAP 2400e.

In addition to high performance processing, the DAP 3400a provides high speed simultaneous analog sampling. The analog section is expandable —see Table 2 for complete specifications.

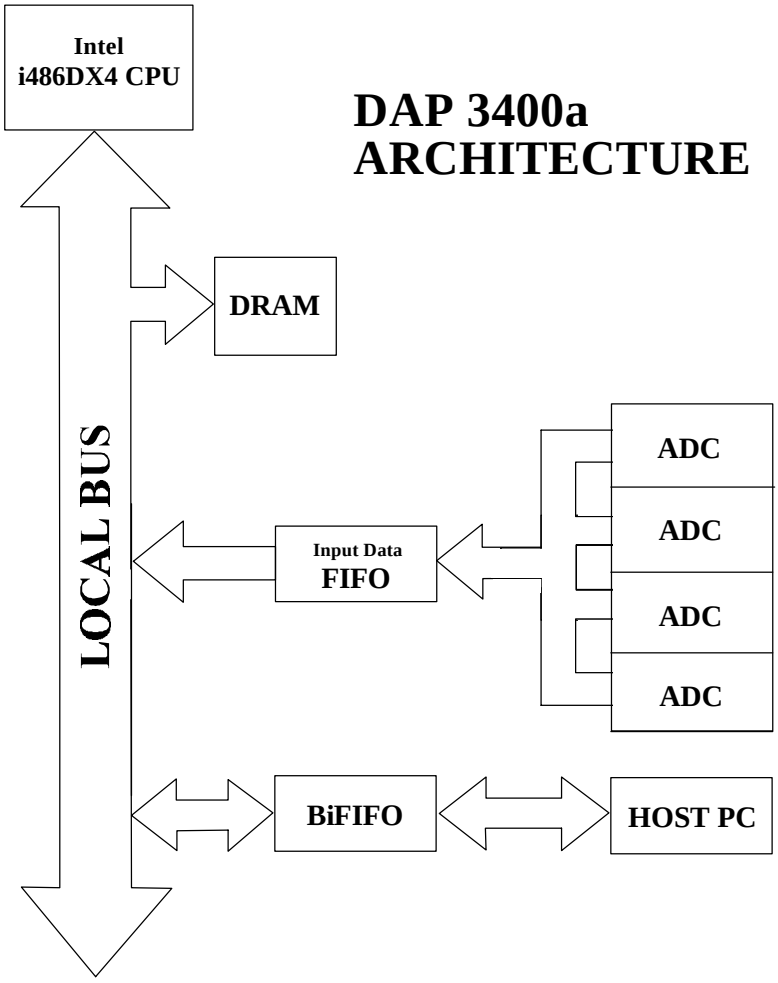

Figure 1: DAP 3400a Data Acquisition Hardware

Figure 1 displays the architecture of the internal processing hardware of the DAP 3400a. The figure shows the two FIFOs on the DAP 3400a that handle data acquisition and communications. The BiFIFO on the DAP 3400a handles communications between the Data Acquisition Processor and the PC. Information can be sent in both directions simultaneously, and can be either DAPL files, binary or text data, error messages, or DAPL system commands. In addition to the BiFIFO for communications, there is an an input data FIFO. The data FIFO is unidirectional, buffering data from the analog inputs.

Data are acquired via dedicated hardware clocking circuitry at a rate of up to 800K samples per second on each of four simultaneously-sampled channels, for an aggregate rate of 3.2 million samples

per second. Acquisition is clocked at a sampling rate controlled in software, and the rate is accurately maintained by onboard crystal-controlled timers. The sample period is specified with a resolution of 50 nanoseconds. The sample rate is accurate to 50 parts per million.

In addition to onboard timing, the DAP 3400a also has provisions for external triggering and clocking for the input section. Software triggering is provided in DAPL, providing pre-trigger as well as post-trigger data and allowing complex trigger events. The DAP 3400a may be synchronized with virtually any other Data Acquisition Processor.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 3400a are given in Table 2.

Table 2: DAP 3400a Typical Hardware Specifications

Specification	DAP 3400a/445
Dimensions	13.33" x 4.8"
Weight	13.6 oz
CPU type	Intel i486 DX4
CPU clock speed	96 MHz
CPU DRAM	8 Mbytes
Cache size	16 Kbytes
Bus support	AT ISA
PC interface hardware	dual 1 KWord biFIFO buffers
PC transfer mode	I/O Interrupt
Maximum transfer rate	816K samples/sec
Power requirements	+5V, 3.5 Amps
Operating temperature	0-50 °C
Accuracy of crystal clocks	50 parts per million
Type of A⇒D converter	Successive Approximation
Max. analog sample rate (four channels per sample)	800 K samples/s per analog-to-digital converter
Max. aggregate sample rate	3.2 M samples/s
Number of analog input channels	16
Expandable To	512
Input voltage ranges	-2.5 to 2.5 V -5 to 5 V
Resolution -5 to 5 V range	12 bits 2.4 mV
Accuracy -5 to 5 range	±1 LSB ±2.4 mV
Non-linearity	0.05%
Input bias current	12 nA
Analog input impedance	>> 10 MΩ
Common mode rejection	90 dB
Max. analog input voltage	±25 V
External clock input min. pulse width	25 ns
External trig. input min. pulse width	60 ns
Trigger modes	GATED ONE-SHOT