MICROSTAR LABORATORIES™

2265 116th Avenue N.E., Bellevue, WA 98004
Sales & Customer Support: (425) 453-2345
Finance & Administration: (425) 453-9489
Fax: (425) 453-3199
World Wide Web: http://www.mstarlabs.com/

Technical Note TN-107 **Version 1.1**

Technical Product Information for the DAP 3216a™

The DAP 3216a

- has an Intel i486DX4 processor onboard
- has 16-bit resolution analog inputs and outputs
- comes with 4MBytes of DRAM onboard memory
- forms the high end of the a-Series Data Acquisition Processor™ boards
- is compatible with other a-Series boards
- works with the PC/AT/ISA bus for 286/386/486 PC or Pentium platforms
- transfers data to PC at high rates — up to 909K samples per second
- allows fast real-time processing
- offers low latency—0.2 ms task time quantum—for fast response
- offers sampling period resolution to 100 ns
- provides onboard DSP routines
- samples or updates the digital section at up to 1.66 million values per second
- samples analog inputs at up to 200K samples per second
- updates analog outputs at up to 500K samples per second each
- has expandable analog and digital inputs/outputs

There is one DAP 3216a ™ model: the DAP 3216a/415. This technical note describes the DAP 3216a in terms of its similarities with other a-Series boards, software speed and functionality, and hardware characteristics.

The DAP 3216a is one of the highest performance Data Acquisition Processors produced by Microstar Laboratories. The DAP 3216a is compatible with other a-Series boards and may be interchanged in any hardware configuration.

The onboard multi-tasking operating system, DAPL™, runs on every Data Acquisition Processor, and ensures that hardware-level differences are transparent. DAPL is a complete software environment for real-time data acquisition. To aid application development, DAPL comes complete with many system diagnostics in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, PID control, fast Fourier transforms, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data aquisition application. Custom commands can also be written with the Developer's Toolkit for DAPL™ if multiple commands need to be combined, or if a specific application cannot be implemented with standard DAPL commands. On the next page, some standard DAPL commands are tabulated with a comparison of their speed of execution on the DAP 3216a/415 and DAP 2416a™/6.

Another common element among a-Series boards is the bus interface. Like every a-Series Data Acquisition Processor, the DAP 3200a is compatible with the PC/AT/ISA bus for 286/386/486 and Pentium platforms. Dual 1K word biFIFO buffers allow fast data transfer to and from the host PC. The maximum transfer rates for the DAP 3200a are 909K samples per second to sample and transfer information to the PC, and 957K samples per second to send information from the PC.

The main differences between the DAP 3216a and other a-Series boards is that the DAP 3216a has 16-bit analog input and output sections. The DAP 3216a is therefore an excellent choice for applications concurrent real-time processing and data sampling, and for applications requiring 16-bit resolution.

The i486 also gives the DAP 3216a low latency: down to a 0.2 ms task time quantum. This means that when low latency mode is enabled, a single task will run for no more than 0.2 ms before DAPL switches to another task. This is crucial for process control applications where data must be responded to as quickly as possible.

Table 1: Comparison of DAPL command speeds —DAP 2416a/6 and DAP 3216a/415

DAPL Command	Description	Time of Execution[1] on DAP 2416a™/6	Time of Execution[1] on DAP 3216a/415
`AVERAGE`	Averages groups of 16 data points[2]	70.4 µs	8 µs
`FFT`	FFT of blocksize of 512 points[2]	5.3 ms	2.0 ms
`RFILTER`	Filters input data with 20 tap filter	9.4 µs	3.2 µs
`LIMIT`	Generates level-based triggers on 1% of data	4.8µs	0.4 µs
`WAIT`	Processes data based on triggers at a retention rate of 5 out of 100 samples	2.4 µs	0.2 µs
DAPL Expression: `P3 = P1 + P2`	Adds two word-length pipe values together	30.8 µs	8.4 µs

[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds for the task are actually smaller.

[2] The speed given is for the entire operation on all data points, including system overhead. Contact Microstar Laboratories for task speed.

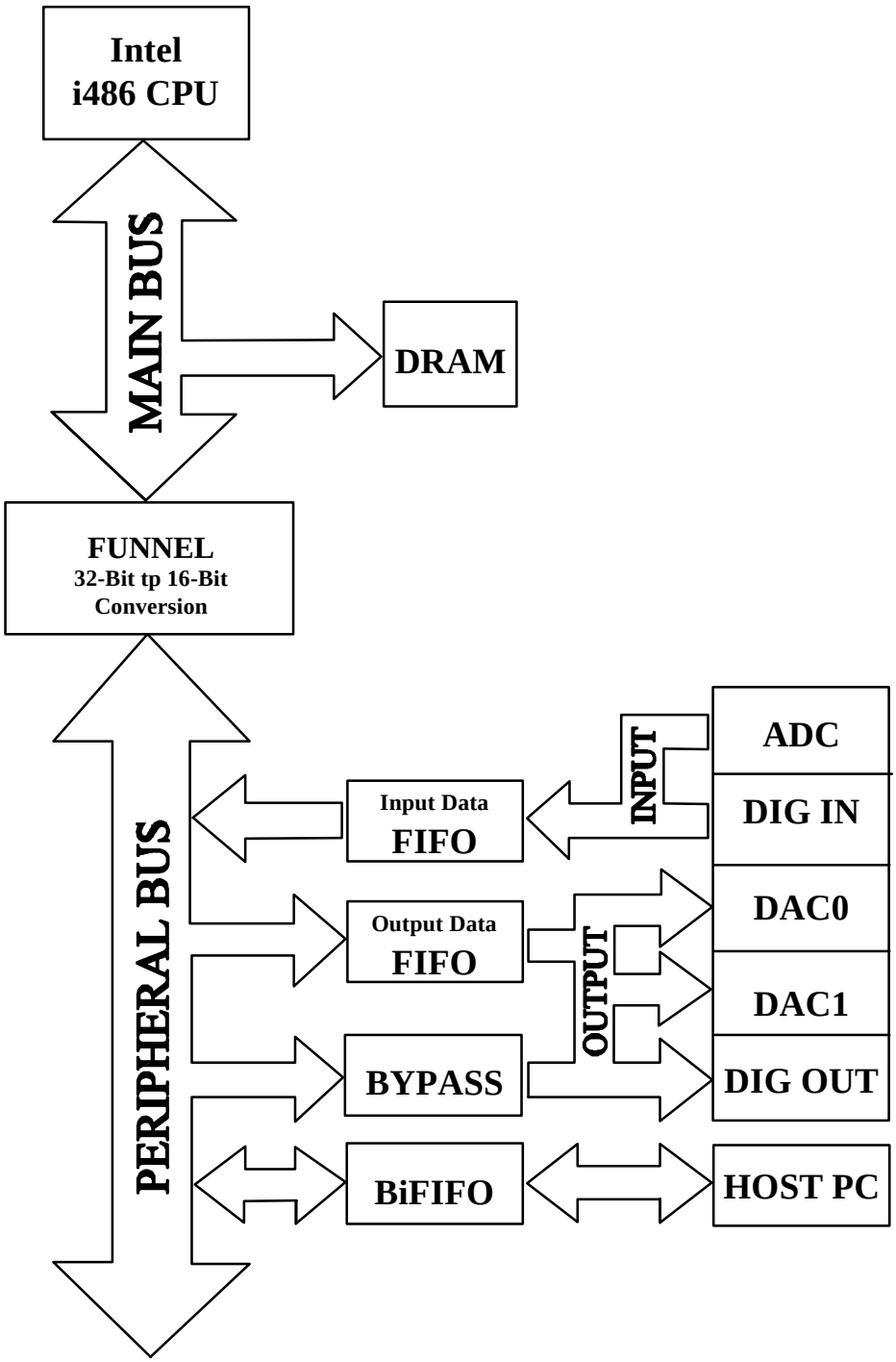

Figure 1: DAP 3216a Data Acquisition Hardware

From the point of view of DSP-intensive applications, the main difference between the DAP 3216a and the DAP 2416a is that, while the DAP 3216a has an i486 processor, the DAP 2416a has a 80C186XL processor and a DSP coprocessor. The DAP 3216a handles DSP routines with the i486 processor instead of the dedicated DSP coprocessor of the DAP 2416a. This may seem slower than using a dedicated DSP coprocessor, but in fact the DAP 3216a/415 is faster than the DAP 2416a in all cases. The i486 processor features a hardware multiplier, just like the dedicated DSP processor has, and the i486 has a large internal cache memory and much higher clock rate so it can actually out-perform the dedicated DSP on the

DAP 2416a. For non-DSP commands the DAP 3216a is even faster; about sixteen times faster than the DAP 2416a. The DAP 3216a is better than the DAP 2416a for virtually every application and is a better value.

In addition to high performance processing, the DAP 3216a provides the standard arrangement of complete analog/digital input and output sections. These analog and digital sections are completely expandable — see Table 2 for complete specifications.

Figure 1 displays the architecture of the internal processing hardware of the DAP 3216a. The figure shows the three FIFOs on the DAP 3216a that handle data acquisition and communications. The BiFIFO on the DAP 3216a handles communications between the board and the PC. Information can be sent in both directions concurrently, and can be DAPL files, binary or text data, error messages, or DAPL system commands. In addition to the BiFIFO for communications, there is an output data FIFO and an input data FIFO. The data FIFOs are unidirectional, buffering data for either input or output.

Data are acquired or updated via dedicated hardware clocking circuitry at a rate of up to 1.66 million samples per second. Acquisition is clocked at a sampling rate or output rate controlled in software, and the rate is accurately maintained by onboard crystal-controlled timers. The sample period is specified with a resolution of 100 nanoseconds. The sample rate is accurate to 50 parts per million.

In addition to onboard timing, the DAP 3216a also has provisions for independent external triggering and clocking for inputs and outputs. This allows for sampling to be triggered from or synchronized with external signals.

The 16-bit digital input port and the analog-to-digital converter are attached to the Input Data FIFO, one of the unidirectional data FIFOs. The maximum aggregate sample rate is 1.66M samples per second. Digital input alone can run at up to 1.66M samples per second. The maximum analog input sample rate is 200K samples per second.

The digital output port and the two analog outputs are attached to the Output Data FIFO. The maximum aggregate update rate is 1.66M updates per second. Digital output alone, like digital input, can run at up to 1.66M updates per second. Each of the analog outputs can be updated at up to 500K updates per second, although at update rates greater than 400K updates per second accuracy is reduced.

The Bypass section shown in Figure 1 allows the 486 processor to asynchronously update either the digital or analog outputs. This means that periodic timing is not guaranteed, rather the 486 processor will attempt to update the outputs whenever a time slice for this task becomes available. This is useful in control application where a digital output, for example, needs to open or close a valve at irregular intervals.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 3216a are provided in Table 2.

Table 2: DAP 3216a Typical Hardware Specifications

Specification	DAP 3216a/415
Dimensions	13.33" x 4.8"
Weight	13.3 oz
CPU type	Intel DX4
CPU clock speed	96 MHz
CPU DRAM	4 Mbytes
Bus support	ISA AT
PC interface hardware	dual 1 KWord biFIFO buffers
PC transfer mode	I/O Interrupt
Maximum transfer rate	909K samples/sec
Power requirements	+5V, 3.0 Amps
Operating temperature	0-50 °C
Accuracy of crystal clocks	50 parts per million
Type of A⇒D converter	Successive Ap-proximation
Model of A⇒D converter	Analog Devices AD976A
Max. analog sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 200 K samples/s 100 K samples/s 17 K samples/s 2 K samples/s
Number of analog channels	16
Expandable To	512
Input voltage ranges	-5 to 5 V -10 to 10 V
Max. input voltage (fault-protected multiplexers)	±25 V
Resolution -5 to 5 V range	16 bits 150 uV
Accuracy -5 to 5 range	±2 LSB ±300 uV
Non-linearity	±2 LSB
Input Noise	±3.5 LSB*
Input bias current	12 nA
Analog input impedance	>> 10 MΩ
Common mode rejection	>98 dB
Type of D⇒A converter	Voltage Output

Model of D⇒A converter	Analog Devices AD669
Maximum analog update rate	500K updates/sec (400K or less for full accuracy)

* Accuracy may be increased by minimizing the input noise. This may be done by filtering data on the Data Acquisition Processor.

Table 2: DAP 3216a Typical Hardware Specifications, continued

Specification	DAP 3216a/415
Number of output channels	2
Expandable to	66
Output ranges	-5 to 5 V -10 to 10 V
Resolution -5 to 5 V range	16 bits 150 uV
Accuracy -5 to 5 V range	±2 LSB, ±300 uV
Analog output temperature drift	±1.5 LSB per ºC
Current source maximum	±1 mA
Digital input/output logic	FCT TTL
Maximum digital update rate[3]	2M words/sec
Number of input bits Number of output bits	16 16
Expandable to	128 input bits and 1024 output bits
Digital input Min. logical high Max. logical low Max. current sink Max. current source	 2 V 0.8 V 5 µA 5 µA
Digital output Min. logical high Max. logical low Max. current sink Max. current source	 2.4 V 0.5 V 12 mA 15 mA
External clock input min. pulse width	25 ns
External trig. input min. pulse width	60 ns
Trigger modes	GATED ONE-SHOT

This figure is the maximum throughput of simultaneous digital input and output. Either digital input or digital output operating alone can maintain a throughput of 1.6 M words/sec.