MSXB 050 Accessory Board Manual

Quadrature Decoder Board

Version 1.10

Microstar Laboratories, Inc.

Microstar Laboratories, Inc.
2265 116th Avenue N.E.
Bellevue, WA 98004
Tel: (425) 453-2345
Fax: (425) 453-3199
www.mstarlabs.com

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MSXB 050: Quadrature Decoder Board

The Microstar Laboratories Quadrature Decoder Board, part number MSXB 050, allows a Data Acquisition Processor to read quadrature-encoded signals. Quadrature encoded signals often are used to measure the angular (rotational) velocity and position of wheels, gears, and motors.

A quadrature encoded signal consists of two digital square waves that are 90° out of phase with each other. The speed of rotation determines the frequency of the square waves, while the direction of rotation determines the phase relationship between the two square waves. The Quadrature Decoder Board decodes quadrature encoded signals and keeps track of the angular position by means of an up/down counter.

The Quadrature Decoder Board has four external input lines. Each counter can measure quadrature encoded signals with frequencies up to 1 MHz and has a counter resolution of 16 bits. The counter resolution can be extended to 32 bits via software. Up to 6 Quadrature Decoder Boards can be used in a system for a total of 24 counter channels.

The Quadrature Decoder Board can be used in conjunction with a Digital Expansion Board to provide digital input and output expansion as well as quadrature inputs. When used in conjunction with digital input expansion, the maximum number of Quadrature Decoder Boards that can be used is reduced to 3, for a total of 12 quadrature counter channels, then one Digital Expansion Board can be used for a total of 64 digital inputs and 64 digital outputs.

All counters on the Quadrature Decoder Board are reset when the Data Acquisition Processor is reset. This occurs each time the DAPL system is downloaded to the Data Acquisition Processor board at power up and under control of the ACCEL32 driver system or application software using certain specialized features of the DAPIO32 programming interface. After the initial reset, applications can use the five external Quadrature Decoder Board reset lines to reset all of the counters as a group or to reset each counter individually. All five reset inputs are pulled to the inactive state internally when no external signal is connected, so it is not necessary to connect the reset inputs if they are not used. A reset signal must be in the active state for at least 400ns to guarantee it will be recognized.

The DAPL system RESET command will not clear the Quadrature Decoder Board counters. Most software configurations contain a RESET command, hence these configurations can be downloaded and started without losing counter information.

Hardware Configuration

Four configurations of the Quadrature Decoder Board are available; two stand-alone configurations, an industrial enclosure configuration, and a single-board enclosure configuration. Each configuration is available as a specific model.

One stand-alone configuration, MSXB 050-xx-C3Z, connects to a Data Acquisition Processor with a 100-line cable adapter board, part number MSCBL 046-01 or MSCBL 076-01 and a 100-line cable, part number MSCBL 054-01 or part number MSCBL 056-01. The MSCBL 046-01 or MSCBL 076-01 attaches to the Digital Input/Output Port of the Data Acquisition Processor. The MSCBL 054-01 or MSCBL 056-01 connects the cable adapter board to connector `J1` of the Quadrature Decoder Board. This model of the Quadrature Decoder Board also may be connected directly to the Digital Input/Output Port of the Data Acquisition Processor with a 100-line adapter ribbon cable, part number MSCBL 058-01.

The other stand-alone configuration, MSXB 050-xx-K3Z, connects directly to a Data Acquisition Processor with a 100-line ribbon cable, part number MSCBL 036-01. MSCBL 036-01 attaches to the Digital Input/Output Port of the Data Acquisition Processor and to connector `J10` of the Quadrature Decoder Board. This is the same connection configuration as MSXB 023 so this option is a good choice when using MSXB 050 as a replacement for MSXB 023.

The industrial enclosure configuration, MSXB 050-xx-E3M, connects to the digital backplane inside an industrial enclosure, which in turn is connected to a Data Acquisition Processor. The industrial enclosure connects to the Data Acquisition Processor by means of a 100-line cable, part number MSCBL 054-01 or part number MSCBL 056-01.

The single-board enclosure configuration, MSXB 050-xx-C3F, connects to the Data Acquisition Processor by means of a 100-line cable adapter board, part number MSCBL 046-01 or MSCBL 076-01 and a 100-line cable, part number MSCBL 054-01 or part number MSCBL 056-01. The MSCBL 046-01 or MSCBL 076-01 attaches to the Digital Input/Output Port of the Data Acquisition Processor. The MSCBL 054-01 or MSCBL 056-01 connects the cable adapter board to connector `J1` of the Quadrature Decoder Board. This model of the Quadrature Decoder Board also may be connected directly to the

Digital Input/Output Port of the Data Acquisition Processor with a 100-line adapter ribbon cable, part number MSCBL 058-01.

Warning: Never connect or disconnect the Quadrature Decoder Board while the Data Acquisition Processor or the Quadrature Decoder Board is powered.

Input Signal Details

The Quadrature Decoder Board provides four independent input channels. Each input channel has two terminals for quadrature encoded signals and two terminals for their corresponding grounds. Connectors `J5`, a Wago type screw terminal block, and `J9`, a male DB-25 connector, provide termination for the counter input signal lines. Connector `J9` also provides termination for all five reset inputs.

The quadrature inputs are Schmitt-triggered CMOS. The positive-going threshold for a "1" input is 4.0V. The negative-going threshold for a "0" input is 1.0V. These inputs have 4.7K pull-up resistors that allow TTL signal drivers to be used. If TTL quadrature signals are applied, the TTL driver must allow its output to be pulled higher than 4V. The quadrature inputs sink no more than 15 microamps for a "1" input and source no more than 1.1 milliamps for a "0" input. Signals may be applied to the Quadrature Decoder Board while the Data Acquisition Processor or Quadrature Decoder Board is off. Fault protection is provided for the quadrature inputs so voltages up to +/-15 Volts may be applied without causing damage.

The reset inputs are TTL-compatible CMOS. The positive-going threshold for a "1" input is 2.4V. The negative-going threshold for a "0" input is 0.8V. These inputs have 10K pull-up resistors and will sink no more than 15 microamps for a "1" input and source no more than 0.6 milliamps for a "0" input. Reset signals may be applied to the Quadrature Decoder Board while the Data Acquisition Processor or Quadrature Decoder board is off. Fault protection is provided for the reset inputs so voltages up to +/-15 Volts may be applied without causing damage.

Warning: Never apply a voltage greater than +15V or less than -15V to a quadrature or reset input.

A quadrature encoded input consists of two square wave signals that are 90° out of phase with each other. These two signals can be described by four states, where the two signal levels are constant in each state. The minimum allowable time period of each state is 200 nanoseconds. The minimum low or high period of each signal is 400 nanoseconds. The minimum period of each signal is 1000 nanoseconds, which corresponds to a maximum frequency of 1 MHz.

Hardware Reset Inputs

Figure 1 shows the location of the connectors and headers on MSXB 050.

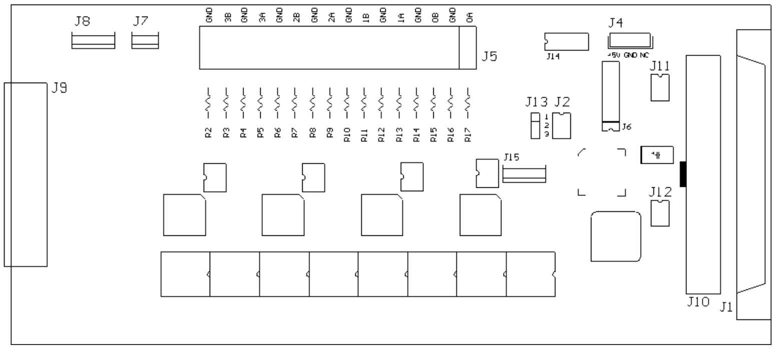
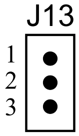


Figure 1. Connector Locations

The polarity of the external reset signals may be selected to be active high or active low. The active polarity of all five external reset signals is selected by the position of a single shunt on header J13. The external reset signals are active high when the shunt is between pins 1 and 2 on J13 and the external reset signals are active low when the shunt is between pins 2 and 3 on J13. The following figure shows the pin-out of header J13:



Shunt Position	Function
1-2	Resets Active High
2-3	Resets Active Low

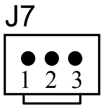
Figure 2. J13 - Reset Polarity Header

When the reset signals are configured to be active low, the counter(s) will be reset when the reset signal is low (less than 0.8V) for at least 400ns. Conversely, when the reset signals are configured to be active high, the counter(s) will be reset when the reset signal is high (more than 2.4V) for at least 400ns.

All five hardware reset signal inputs are available on input connector J9. Additionally, the global reset signal that resets all four counters is available on connector J7 and the four individual-counter reset signals are available on connector J8. The signal named Reset is used to reset all counters at the same time. The signal named Reset0 is used to reset counter 0, Reset1 is used to reset counter 1, and so on.

Connector J7 is a 3-pin Molex header, Molex part number 22-23-2031. The mating connector is Molex part number 22-01-3037 which uses crimp pins 08-50-0114.

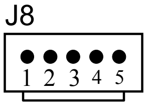
The pin-out of J7 is such that a shunt may be used to reset all counters when the resets are configured to be active low. Placing a shunt between pins 1 and 2 when the resets are configured to be active low will reset all counters; removing the shunt releases the counters from reset. Placing a shunt between pins 1 and 2 has no effect when the counters are configured to be active high. The following figure shows the pin connections for J7:



Pin	Signal
1	Ground
2	Reset
3	N/C

Figure 3. J7 - Global Reset Input Connector

Connector J8 is a 5-pin Molex header, Molex part number 22-23-2051. The mating connector is Molex part number 22-01-3057 which uses crimp pins 08-50-0114. The following figure shows the pin connections for J8:



Pin	Signal
1	Ground
2	Reset0
3	Reset1
4	Reset2
5	Reset3

Figure 4. J8 - Individual Counter Reset Input Connector

Connector J9 is a male DB-25 connector that protrudes through the front panel of MSXB 050 models that are mounted in an enclosure. J9 also is easily accessible on MSXB 050 models that are not mounted in an enclosure. All quadrature and reset inputs are available on J9 along with signal ground and a limited amount of +5VDC power. No more than 500mA may be drawn from the +5VDC power pin. The following figure shows the pin connections for J9:

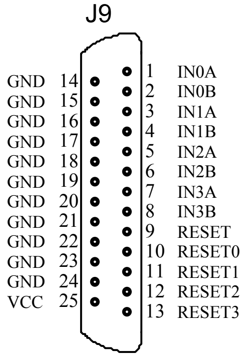


Figure 5. J9 - Input Connector

The quadrature inputs also are available on `J5`, a Wago screw terminal block. The following figure shows the pin connections of `J5`:

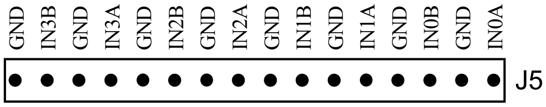


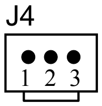
Figure 6. J5 - Input Terminal Block

More Than One Quadrature Decoder Board

The industrial enclosure configuration is the best option for systems with more than one Quadrature Decoder Board or when other external boards are used with one or more Quadrature Decoder Boards. An industrial enclosure provides secure, high-density mounting for multiple Quadrature Decoder Boards with simple cabling and power connection.

If more than one Quadrature Decoder Board in the stand-alone or single-board-enclosure configuration is used in a system, a daisy-chain cable must be used. The daisy-chain cable connects the J1 or J10 connectors of all Quadrature Decoder Boards together. No daisy-chain cable is required for multiple Quadrature Decoder Boards in the industrial enclosure configuration.

If more than three Quadrature Decoder Boards in the stand-alone or single-board-enclosure configuration are to be connected to a Data Acquisition Processor, an external power supply is required. Power from the Data Acquisition Processor must be disconnected before an external power source may be connected to the Quadrature Decoder Board. Headers J11 and J12 allow power from the Data Acquisition Processor to be disconnected; remove all shunts from J11 and J12 to disconnect power from the Data Acquisition Processor. When all shunts have been removed from J11 and J12, an external power supply may be connected to connector J4 on the Quadrature Decoder Board. Each Quadrature Decoder Board draws about 0.6 Amp at +5 volts. Connector J4 is a 3-pin Molex header, Molex part number 26-60-4030. The mating connector is Molex part number 09-50-3031 which uses crimp pins 08-50-0106. The following figure shows the pin connections for J4:



Pin	Signal
1	+5 Volts DC
2	Ground
3	N/C

Figure 7. J4 - External Power Input Connector

Note: In many applications it is convenient to power the Quadrature Decoder Board from the host PC’s power supply.

The industrial enclosure itself must be powered externally if more than three Quadrature Decoder Boards are used in an industrial enclosure. This is because the Data Acquisition Processor can not provide sufficient power due to limitations of the ISA or PCI bus in the PC. In this case the industrial enclosure may be powered by a spare disk drive power connection in the PC or by an external power supply. In this configuration, the Quadrature Decoder Boards in the industrial enclosure do not require special power configuration because they are powered by the industrial enclosure rather than directly from the Data Acquisition Processor. So in the industrial enclosure configuration all shunts remain in place on `J11` and `J12`.

Address Range

There are three address shunts on the Quadrature Decoder Board. These shunts allow multiple Quadrature Decoder Boards to be used with one Data Acquisition Processor. These address shunts are located on header J2. The following figure shows the pin numbering of header J2:

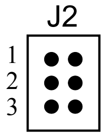


Figure 8. J2 - MSXB 050 Address Selection Header

The board address determines the address of both the control port and the data port. The board address is selected by installing shunts on header J2 as shown in the table below:

Table 1. MSXB 050 Address Configuration

Hardware Board Address	**Jumpers**	**Software Control Port**	**Software Data Port**
0	1, 2, 3	B3	B0
1	1, 2	B3	B1
2	1, 3	B3	B2
3	1	Not valid	Not valid
4	2, 3	B7	B4
5	2	B7	B5
6	3	B7	B6
7	none	Not valid	Not valid

The control port address can be shared by up to three Quadrature Decoder Boards. The control port has two hardware selectable addresses: B3 and B7. The data port address ranges from B0 through B7 except B3 and B7. When using multiple Quadrature Decoder Boards, each board must have a unique data port address.

Software Configuration

As seen from the Data Acquisition Processor, the Quadrature Decoder Board consists of two input ports: a control port and a data port. Reading the control port latches (stores) values of all the counters on the Quadrature Decoder Board for reading. Internally, the counters continue to monitor and count events, while latched values remain stable. After latching, each operation reading from the data port obtains one latched counter value. The first read from the data port obtains the latched value from the first counter. Subsequent read operations obtain the latched count values from the second, third and fourth counters in sequence. Reading the control port again ends the read sequence and latches new count values in all channels. Reading the data port again begins the next cycle of reading counter values, starting with the first counter.

For example, the following DAPL input sampling configuration reads the Quadrature Decoder Board counters for a board assigned to digital port B0. For an input port in the range B0 to B2, the control port is at address B3.

```
IDEF Quad4In
  CHANNELS  5
  SET IPIPE0 B3   // Latch all counters
  SET IPIPE1 B0   // Read value of counter 0
  SET IPIPE2 B0   // Read value of counter 1
  SET IPIPE3 B0   // Read value of counter 2
  SET IPIPE4 B0   // Read value of counter 3
  TIME 10
END
```

Reading from control port B3 does not obtain useful data, it merely latches all counter values. Reading from the assigned data port, four times, yields readings from the board's four counters. This example shows a time interval of 10 microseconds between readings, but the minimum sampling period is 1 microsecond.

The counter registers must be read in order, hence skipping channels is not allowed. However, not all counters must be read. For example, the following configuration reads only the first two counters, and omits the last two.

```
IDEF Quad2In
  CHANNELS  3
  SET IPIPE0 B3  // Latch all counters
  SET IPIPE1 B0  // Read value of counter 0
  SET IPIPE2 B0  // Read value of counter 1
  TIME 10
END
```

In the next example, two Quadrature Decoder Boards are used to monitor six counter channels. The first board address is set to B0 and the second board address is set to B1. Both of these boards respond to the same control port address B3, so only one data latch operation is needed to latch the counts on both boards. Four counter values are obtained from the first Quadrature Decoder Board. The remaining two counter values are obtained from the second board. Note that counters are read in ascending order on each board. A "dummy" read operation is added so that the channel list is scan is completed in 20 microseconds.

```
IDEF QuadIn 7
  SET IPIPE0 B3   ; Latch counters, both boards
  SET IPIPE1 B0   ; Board 0, read counter 0
  SET IPIPE2 B0   ; Board 0, read counter 1
  SET IPIPE3 B0   ; Board 0, read counter 2
  SET IPIPE4 B0   ; Board 0, read counter 3
  SET IPIPE5 B1   ; Board 1, read counter 0
  SET IPIPE6 B1   ; Board 1, read counter 1
  SET IPIPE7 G    ; Ground, timing adjustment
  TIME 2.5
END
```

Useful Processing Commands

The QDCOUNT and CTRATE commands provided by the DAPL system are often helpful for processing the counts captured by a Quadrature Decoder Board. For complete information about these commands, see the *"DAPL Commands"* chapter of the *DAPL 2000 Manual*.

It is not unusual for the counts accumulated by the Quadrature Decoder Board to exceed the range of the 16-bit internal hardware count register. When that happens, there is a *numerical overflow* condition, and the count appears to jump instantaneously from a large positive value to a large negative value, or the reverse. To avoid the confusion that this can cause, you can apply the QDCOUNT command.

QDCOUNT

The QDCOUNT processing command maintains a 32-bit representation of the running count, compensating for the *numerical overflow* conditions, yielding a running 32-bit count with vastly larger effective range. It also provides some helpful features for establishing the initial state of your processing. Use one copy of the QDCOUNT command for each counter channel that you process.

An additional 32-bit pipe is needed to receive adjusted count values. Suppose that you use four counters, with the counts sampled into logical input channels IP1 through IP4. You can define:

```
PIPES  PC1 LONG, PC2 LONG, PC3 LONG, PC4 LONG
```

You can then convert your 16-bit count values into 32-bit count values in the DAPL processing section, in the following manner:

```
PDEFINE  PROCESSING
  QDCOUNT(IP1,PC1)
  QDCOUNT(IP2,PC2)
  QDCOUNT(IP3,PC3)
  QDCOUNT(IP4,PC4)
END
```

Each time a value is received from a timer channel, the corresponding 32-bit accumulated count is updated and placed into the corresponding 32-bit pipe.

There are some additional useful features. You might sometimes want counts to start at a specified initial offset. To use this feature, simply provide the initial count as an optional second parameter, after the input data pipe. In the following example, there is one counter channel, and an initial offset of 16200 counts is desired. Initialize the 32-bit counter as follows.

```
PDEFINE  PROCESSING
  QDCOUNT(IP1, 16200, PC1)
END
```

Another useful feature is the optional operating mode. Most of the time, counters accumulate an arbitrary and unknown number of counts between the time that the hardware counters are initialized and the processing begins. These counts don't matter. What is important is how much the counts change after processing is started. This is the default operating mode, but you can request it explicitly by including the "RELATIVE" keyword string after the optional initial offset specification. The following example does not use an initial value specification , but it does specify the "RELATIVE" operating mode.

```
    QDCOUNT(IP1, “RELATIVE”, PC1)
```

On the other hand, sometimes counts are initialized according to a hardware synchronizing signal, and then it is important to capture all counts from that time onward. For this case, you should initialize the hardware first, and then immediately start software processing, specifying the "ABSOLUTE" mode.

```
    QDCOUNT(IP1, “ABSOLUTE”, PC1)
```

A QDCOUNT Application Example

A precision positioning application uses a worm drive gear mechanism, monitored by an optical quadrature encoder. There is a reference location established beyond the ordinary range of motion. After calibration, it is known that exactly 8200 counts of displacement will move the mechanism to the desired starting position relative to the reference. Hence the absolute position count is not important, but what matters is displacement from the position established by the reference surface.

To start the system, first the device is positioned until it is in contact with the calibrated reference surface. While holding this position, processing is started. The 32-bit position count is initialized at –8200 in the "RELATIVE" operating mode. The actual hardware register count at this moment does not matter. The device can then be commanded to advance to the desired start position, relative to the reference position. When a count of 0 is indicated by the 32-bit running sum, the starting position has been reached.

This application needs a 32-bit pipe for the running count. The input sampling configuration samples only the control port and one counter. We want to assign the logical 32-bit count such that it has an initial value of -8200 while the mechanism is driven against the reference surface. The Quadrature Decoder Board is assigned to port address 0.

We can use the following DAPL configuration for this application:

```
PIPES  PAXIS  LONG

IDEFINE  QDSAMPLE
  CHANNELS  2
  SET  IPIPE0  B3  // Latch counter data
  SET  IPIPE1  B0  // Read latched counter value
  TIME  50
END

PDEFINE  AXIS_MONITOR
  QDCOUNT(IP1,-8200, "RELATIVE", PAXIS)
END
```

After this configuration is running, the positioning device can be commanded to advance the axis to the desired start position. The mechanism has reached the starting position when the Quadrature Decoder count equal to zero.

CTRATE

The CTRATE command computes differences between successive counter values. Because the counter values are captured at regular and equal time intervals, the number of counts change per update is a measure of "speed." Like the QDCOUNT command, the CTRATE command is not confused by *numerical overflow*.

The CTRATE command was originally intended for event counter/timer boards such as the MSXB036. The counter/timer boards are not bidirectional. However, the CTRATE command works equally well with the Quadrature Decoder Board, which is bidirectional.

Suppose that in the previous example a change of more than 320 counts between samples indicates an overspeed condition. We can use CTRATE to monitor the rate of change, and use the ALARM command to asynchronously flag digital output port bit 5 if the rate gets too high.

We can modify the processing configuration from the previous example as follows:

```
PIPE  PRATE WORD
CONSTANT DIGITAL5 WORD = 5

PDEFINE  AXIS_MONITOR
  QDCOUNT(IP1,-8200, “RELATIVE”, PAXIS)
  CTRATE(IP1,PRATE)
  ALARM(PRATE, OUTSIDE,-320,320, DIGITAL5, 1000)
END
```

Using Counters in Custom Programming

Processing code in customized command modules can employ the same software techniques as the QDCOUNT and CTRATE commands for processing a Quadrature Decoder Board counter data stream.

The C++ programming language doesn't provide a direct way to detect integer overflow conditions. However, if counter values do not change more than plus or minus 32767 counts from one reading to the next, the difference between two successive counter readings will always be correct in sign and magnitude, regardless of whether an overflow condition occurred in the 16-bit hardware register. To apply this fact, define some 16-bit integer working variables:

```
short int   prev_val = 0;
short int   next_val;
short int   diff_val;
long  int   accumulator = 0L;
```

After reading each new 16-bit count value, compute the difference with the previous value.

```
next_val = pipe_get(pInput);
diff_val = next_val - prev_val;
```

Then update the 32-bit accumulator, and also update the previous value variable for the next pass.

```
accumulator += (long) diff_val;
prev_val = next_val;
...
```

This is the essence of what the QDCOUNT and CTRATE commands do. Using this technique, you can perform the same kinds of calculations inline as needed to optimize your processing code.