MSXB080 / MSXB081 / MSXB082 Signal Interface Module Manual

Isolated Analog Input Module with Simultaneous Sampling

Version 1.00

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Part Number MSXB080M100

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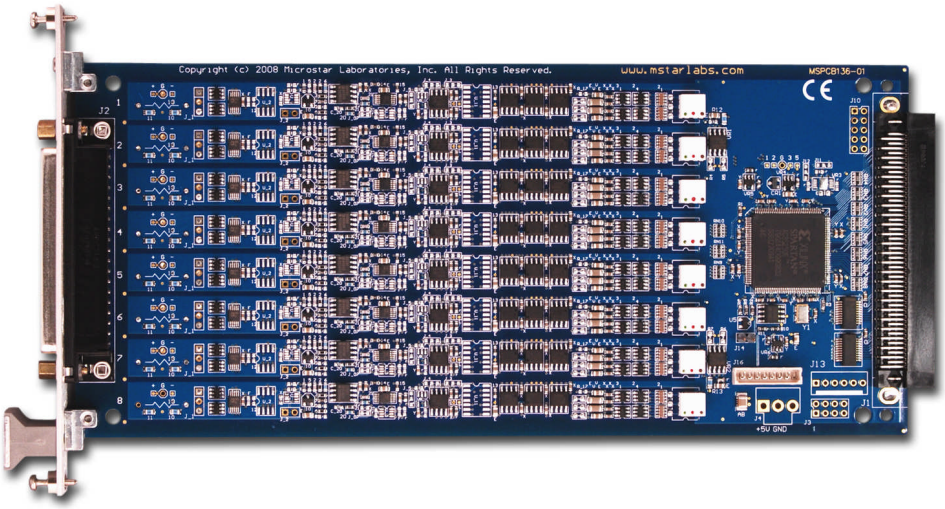

This manual describes three isolated analog input modules, model numbers MSXB080, MSXB081, and MSXB082. They are part of the signal interface (SI) modules by Microstar Laboratories. All three models support different analog inputs with individual 16-bit analog-to-digital converter per channel for simultaneous sampling. They have 300V of channel-to-channel and channel-to-ground isolation. The gains are selectable per channel in software. The MSXB081 supports current inputs between 4-20 mA, with a 20% over-range of up to 24mA. The specifications of the three modules are shown in Table 1.

Up to eight input modules can be connected to one DAP board for 64 isolated analog inputs with the MSXB080 and MSXB081 or 32 inputs with the MSXB082. They can be used with other SI modules, such as isolated analog outputs and isolated digital I/O, in a system. Contact your Microstar Laboratories representative to discuss your needs.

Table 1. Specifications of the isolated analog input modules

	MSXB080	MSXB081	MSXB082
Number of Inputs	**8**	**8**	**4**
Input Range	**+/-10V**	**4-20 mA**	**+/-10V**
Maximum sample rate (kS/s)			
per channel	**333**	**333**	**1000**
aggregate	**2000**	**2000**	**2000**
A/D converters/resolution (bits)	**8 / 16**	**8/ 16**	**4/ 16**
Gains	**1, 2, 5, 10**	**10**	**1, 2, 5, 10**
Isolations (V)*	**300**	**300**	**300**

*Contact Microstar Laboratories for higher isolation requirements.

Hardware Architecture

System Configuration

The backplane model of the modules connects directly to the digital backplane (MSXB034 or MSXB035) of an industrial enclosure or a DAPserver. This allows one or more analog input modules, or other digital expansion boards, to be installed in an industrial enclosure and be connected to one DAP board. The digital interface board (MSXB033) in the enclosure then connects to the DAP board via a MSCBL076-01 and MSCBL054.

Other models are available. Contact your Microstar Laboratories representative to determine all available models.

Note: The backplane model of the module should not be connected or disconnected to the digital backplane while the digital backplane is powered.

Power Requirements

Each module typically requires 200 mA at +5 Volts DC. The Data Acquisition Processor can typically supply 1.5A to 2.0A at +5 Volts. The total power consumption of all modules must not exceed the power availability of the Data Acquisition Processor. Please refer to the hardware documentation of the Data Acquisition Processor for more specific power availability information. If the total power consumption exceeds the power availability of the Data Acquisition Processor, then external power must be used.

Isolation

The analog input modules are designed for 300V of channel-to-channel and board-to-ground isolation. It better protects the analog inputs from noise and eliminates ground loops. As Figure 1 and Figure 2 show, only the digital signals are transferred across the isolation barrier. The diagram for the MSXB082 is the same as that for the MSXB080, except that the MSXB082 has four channels instead of eight.

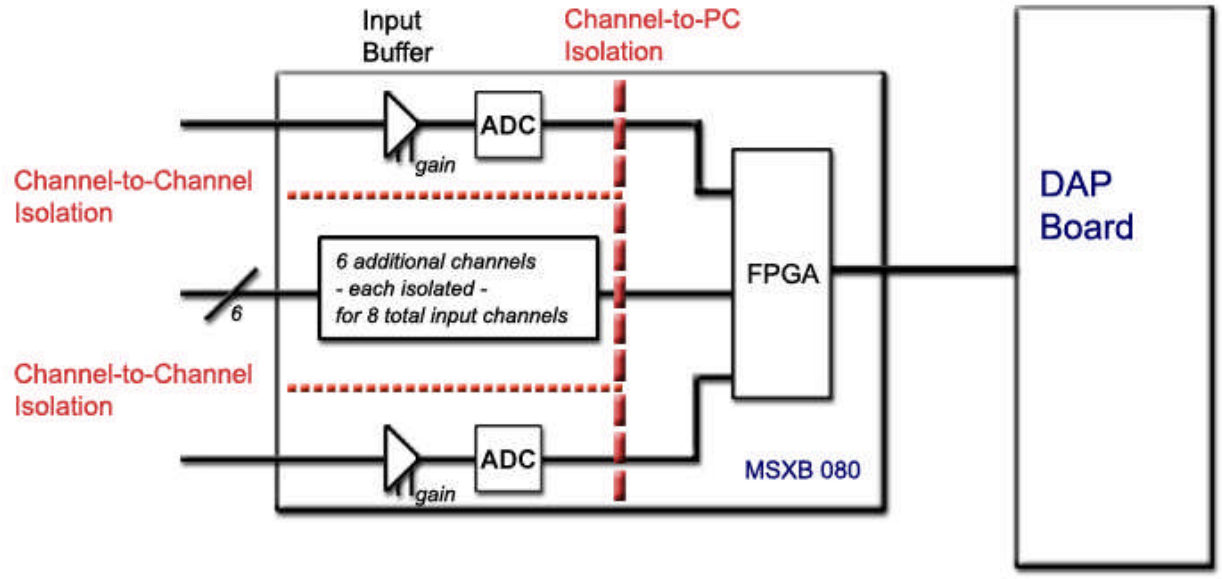

Figure 1. Isolation of MSXB080

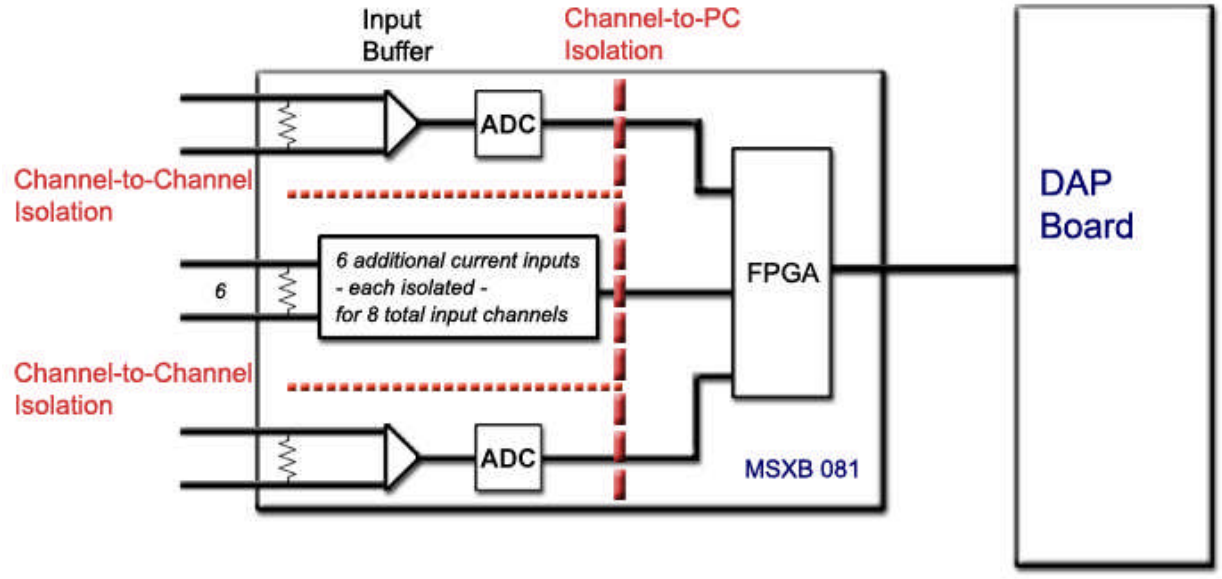

Figure 2. Isolation of MSXB081

Board Layout

The modules are a 3U board measuring 100 mm by 220 mm, or 3.93” by 8.78”. The following diagrams show the layout of the module.

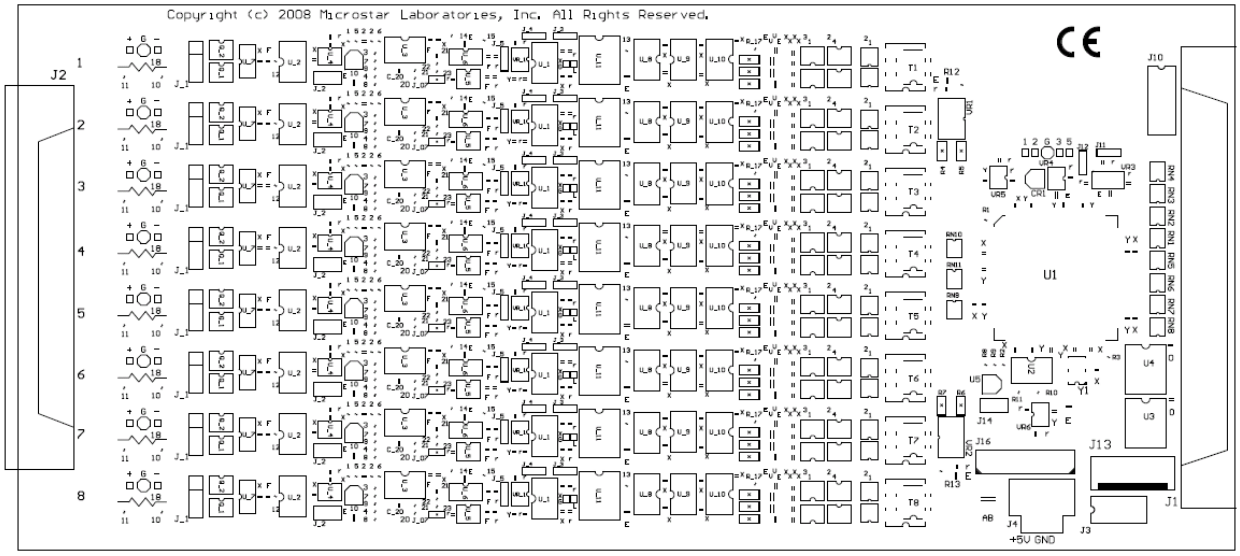

Figure 3. Layout of the MSXB080

Figure 4. Dimensions of the module

Input Connector Options

Input signals can be connected to the analog input modules via the DB37 male connector at J2 or the three-pin headers J_1 for connecting BNC connectors, Lemo connectors, etc.. Each input module is built with either option. The pinouts of the DB37 connector (looking into the connector) and the header are shown below. The DB37 male connector mates with the discrete wire cable kit, part number MSCBL092-01K.

The MSXB082 has four inputs. The pins for D4 to D7 are not connected on its connectors.

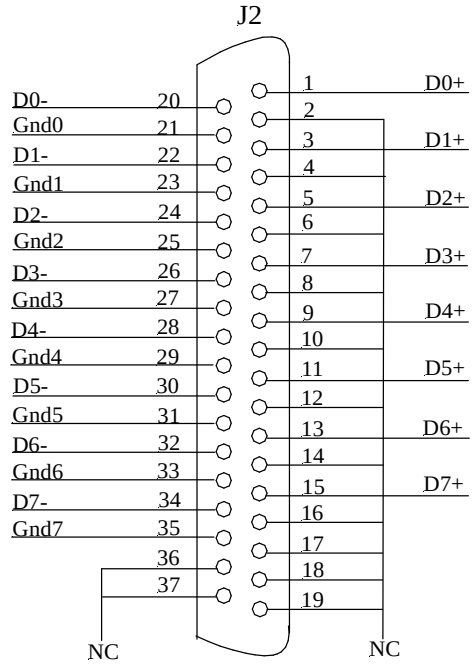

Figure 5. DB37 input connector J2

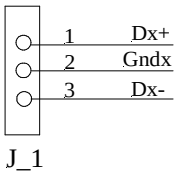

Figure 6. Three-pin header J_1

Software Configuration

The modules are configured by the Signal Interface Module configuration utility. The parameters are listed below:

- Module ID
- Gains
- Channel list
- Addresses – input, scan reset, and sampling

The utility is available for download at www.mstarlabs.com. Refer to the utility manual for more information on the interface.

Hardware Setup

To configure a module, it should be connected to a DAP board that has been installed with Accel32 or DAPcell Server. A new module needs to be initialized by using the configuration utility to add it by its serial number. Refer to the utility manual for instructions.

Module ID

Each module must have a unique Module ID ranging from 1 to 254. The Module ID is used to configure the input and output addresses with the utility program. It can be changed using the utility program. The default Module ID is 255 and the module needs to initialized before it is detected. If two or more modules have the same Module ID, the results are unspecified.

Gains

The MSXB080 and MSXB082 modules have a gain amplifier for each input; the gain is selectable per input. The valid gains are 1, 2, 5, and 10, with the unity gain as the default. The gains are specified at the configuration utility. Each channel in the channel list can only have one gain. MSXB081 has a non-selectable gain of 10 for all eight channels.

Channel List

A channel list is the list of selected inputs in the sequence in which they are read by a DAP board. By default, each read operation of the input address of an input module returns a value from one input in the channel list in sequence. The configuration utility allows the selection of only the inputs that should be returned to the PC. **The number of input pipes sampled in the DAPL configuration must be the same as the number of channels in the channel list.**

The configuration utility in Figure 5 shows a channel list of 15 channels and the sampling sequence.

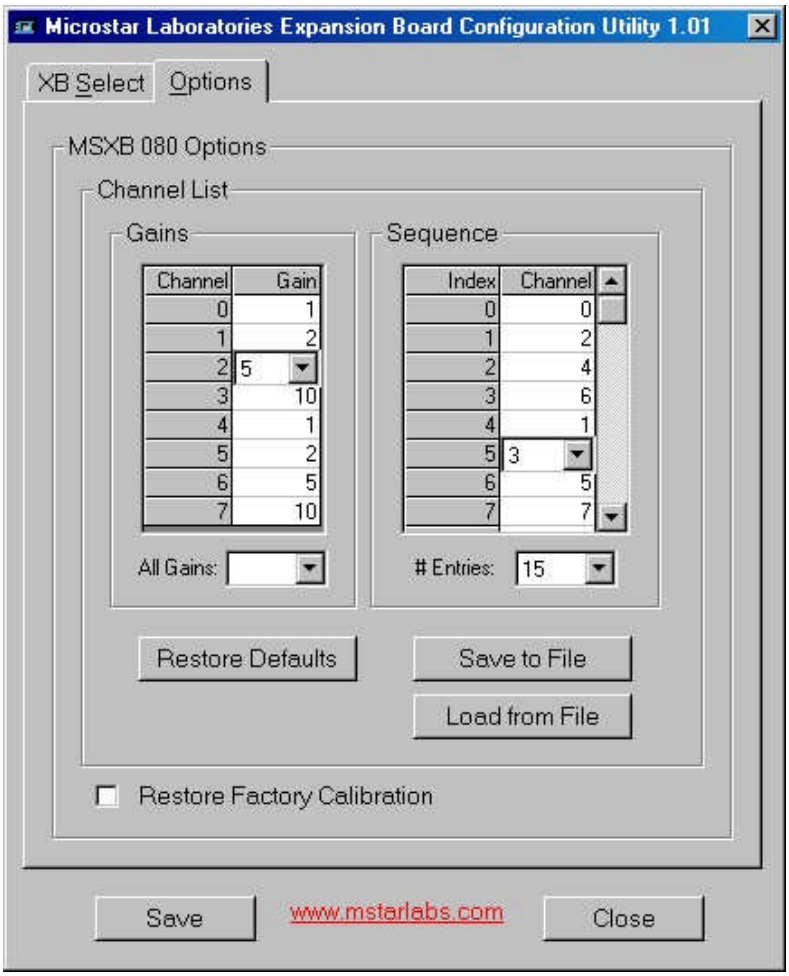

Figure 7. Channel list of a MSXB080 module.

The selection for '# Entries' specifies the number of channels in the sequence. The MSXB080 module has eight inputs in hardware and it can sample an input more than once through the channel list. The figure above shows a list of fifteen channels and the first eight, in sequence, are D0, D2, D4, D5, D1, D3, D5, and D7. The '# Entries' can go up to 64.

Input Address

Each input module should have a unique input address; no two modules can have the same input address. The input address is used for the eight inputs per MSXB080 or MSXB081 and the four inputs per MSXB082. In a DAPL configuration, each operation reading from the input address obtains one data value from the channel list specified in the configuration utility. A maximum of eight modules can be connected to one DAP board. The default input address is B1.

SI Module with Older Analog Input Boards

If the module is used in a system with analog input board(s) connected to the analog I/O port of the same DAP board, avoid using the address B0 as the input or sampling address. When the DAP board samples the analog port, it clears the digital input expansion lines, which causes B0 to sample its inputs.

Scan Address

The input module does the following at the transition to the scan address in a DAPL input definition:

- Latches the values taken at the last read of the scan address and puts the first word value onto the output,
- Starts an acquisition cycle on the eight channels (or four channels), and
- Resets the channel list.

The scan address should be read at a minimum time interval of 3.0 microseconds. The default scan address is B7.

When the system has only one module, the scan address must be different from the input address because it is the transition to the scan address that causes the sampling. If the two addresses are the same, there is no transition to the scan address and thus no sampling of the channels. The single module must be selected to return an input channel for the scan address. If the system has multiple modules, the modules should have the same scan address and the scan address can be the same as one of the input addresses.

For the module that is selected to return an input channel for the scan address (i.e. Sample Returns Input checked), it returns a data value to the DAP board when the scan address is read, as well as when its input address is read. Since reading the scan address returns one channel for that module, its input address should be read one time fewer than the number of channels in the channel list. The examples in the DAPL Configuration section illustrate the different hardware settings.

Since the scan address latches the values read at the last read, there is always a pipeline delay of one scan. The data from the first two passes through the input pipe list in the DAPL input definition should be discarded because they are not valid data. See example #1 in the DAPL Configuration section.

Sampling Address

The transition to the sampling address latches the previous values and puts the first word value onto the output of the module for transfer to the DAP. It does what the scan address does, except that it does not reset the channel list. For most applications, the scan address should be used and the sampling address should be at its default value of OFF. It might be used in an application where some channels need to be sampled at a higher rate than others. See example #5 in the DAPL configuration section.

Timing Diagram

The diagram below illustrates how the scan address and input address affect the channel list and sampling. It shows the sampling clock on the DAP and the 20MHz internal clock on the module after a few passes through the input pipe list in DAPL.

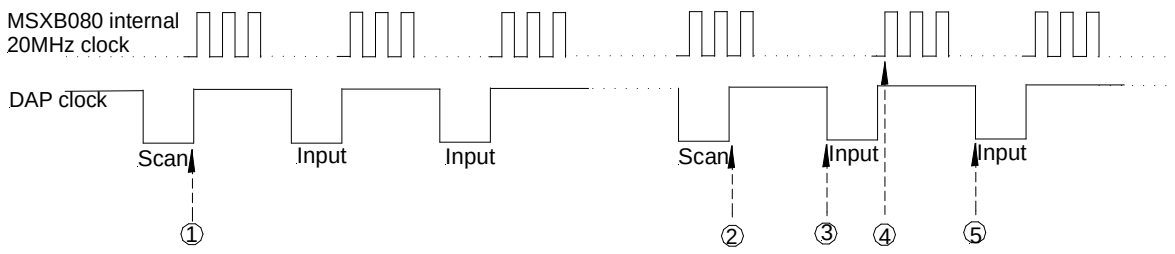

Figure 8. Timing diagram for scan and input addresses

1. The transition to the scan address latches previous values, puts the first word value onto the output, starts conversion on the eight channels, and resets the channel list.

2. Reading the scan address latches the values sampled at time ① and puts the first value onto the output for transfer to the DAP.

3. The DAP reads a value from the scan address at the falling edge of its clock. This value is the first channel on the channel list taken in the last scan, time ① in this case, for the module that is selected to return an input channel for the scan address. That module responds to both the scan address and its input address.

4. The module updates the channel list (i.e. goes to next channel) and puts the next data value sampled at time ① onto the output.

5. The DAP reads a value from the input address at the falling edge. This value is the second channel on the channel list taken at time ① for the module for the corresponding input address.

DAPL Configuration

In this section we will show the DAPL configurations for several hardware settings. The examples describe the MSXB080, but they also work for the MSXB081 and MSXB082.

Example #1 – One MSXB080 Module

The system has one MSXB080 connected to a DAP board with the default settings:

Module	*Input Address*	*Scan Address*	*Sampling Address*	*Sample Returns Input*
MSXB080	1	7	OFF	YES

With one MSXB080 module in the system, the scan address must be different from the input address to have a transition that causes the sampling of the channels. Assume the channel list has the first five inputs D0 to D4 selected. Consider the following DAPL configuration:

```
RESET
IDEFINE MslInputs
   CHANNELS 5
   SET IPIPE0 B7          // Latches the previous values, resets the channel list, and returns data for D0
   SET IPIPE1 B1          // D1
   SET IPIPE2 B1          // D2
   SET IPIPE3 B1          // D3
   SET IPIPE4 B1          // D4
   TIME 10                // sample clock at 10 microseconds, or 50 microseconds per channel
   END
PDEFINE MslProc
   SKIP(IPIPE(0..4), 10, 1, 0, $BINOUT)        // or MERGE(IPIPE0, IPIPE1, IPIPE2, IPIPE3, IPIPE4, $BINOUT)
   END
```

The scan address is sampled at an interval of 50 microseconds, which means the MSXB080 samples the five channels simultaneously at 20 kHz. The DAP board polls data from the MSXB080 module one channel at a time, in the order specified in the channel list. In this example, the order is D0, D1, D2, D3, and then D4.

Since there is only one MSXB080 module in the system, it must be selected to return an input channel for the scan address. That means reading the scan address B7 returns the first channel in the channel list, which is D0 in this example, from the last scan. Note that the input address B1 is read four times, which is one fewer than what you would expect for reading five channels in the channel list. The timing diagram for this example is shown below:

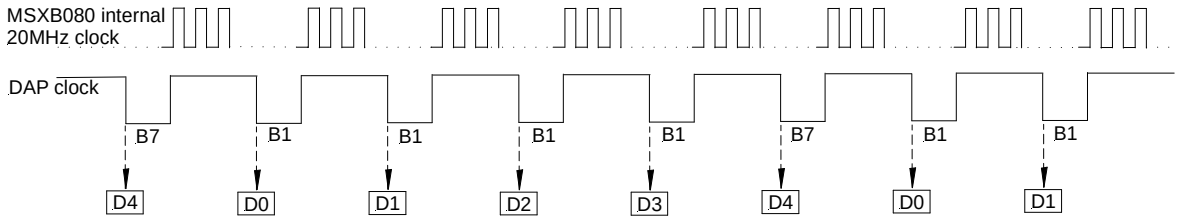

Figure 9. Timing diagram for sampling one MSXB080 module

The first pass through the input pipe list returns no valid data because there is no transition to the scan address to start sampling. The second pass returns data that are from the previous scan, which is at an unknown state. If each and every sampled value from the channels is important, the data from the first two passes of the input pipes should be discarded. The SKIP command shown makes an initial skip of ten samples, or two samples per channel for the five data channels, and then transfers data continuously from the input pipes to the PC via the communication pipe $BINOUT. If the channels are monitored continuously and the first two samples from each channel can be ignored, the channels can be transferred to the PC directly using the MERGE or COPY command.

Example #2 – Two MSXB080 Modules

Consider a system with two MSXB080 modules with the following settings:

Module	*Input Address*	*Scan Address*	*Sampling Address*	*Sample Returns Input*
MSXB080 #1	1	1	OFF	YES
MSXB080 #2	2	1	OFF	NO

The two modules have unique input addresses. The scan addresses should be the same and are equal to one of the two input addresses. MSXB080 #1 is specified to return an input channel for the scan address, which means reading the scan address will return the first channel on its channel list.

Assume that the channel list for each module has the first four channels D0 to D3. The DAPL configuration for sampling the eight channels is shown below.

```
RESET

IDEFINE MslInput
   CHANNELS 8
   SET IPIPE0 B1          // resets the list, returns D0 on module #1,
   SET IPIPE1 B1          // D1 on module #1
   SET IPIPE2 B1          // D2 on module #1
   SET IPIPE3 B1          // D3 on module #1
   SET IPIPE4 B2          // D0 on module #2
   SET IPIPE5 B2          // D1 on module #2
   SET IPIPE6 B2          // D2 on module #2
   SET IPIPE7 B2          // D3 on module #2
   TIME 10                // sample clock at 10 microseconds, or 80 microseconds per channel
   END

PDEFINE MslProc
   SKIP(IPIPE(0..7), 16, 1, 0, $BINOUT)
   END
```

The channels are sampled at 12.5 kHz per channel, with the eight channels on each module sampled simultaneously. As in example #1, the SKIP command discards data from the first two passes of the input pipe list.

Example #3 – Eight MSXB080 Modules

Consider the hardware setting below for a system with eight MSXB080 modules connected to one DAP board.

Module	*Input Address*	*Scan Address*	*Sampling Address*	*Sample Returns Input*
MSXB080 #1	0	0	OFF	Yes
MSXB080 #2	1	0	OFF	No
MSXB080 #3	2	0	OFF	No
MSXB080 #4	3	0	OFF	No
MSXB080 #5	4	0	OFF	No
MSXB080 #6	5	0	OFF	No
MSXB080 #7	6	0	OFF	No
MSXB080 #8	7	0	OFF	No

All the modules have unique input addresses and the same scan address. Since B0 is used, the system should not have any analog input board(s) connected to the DAP via the analog I/O port. Assume that the channel list of each module has two channels. The DAPL configuration for sampling the 16 channels for the eight modules is shown below.

```
RESET
IDEFINE MslInput
   CHANNELS 16
   SET IPIPE0 B0          // 1st channel in channel list on module #1, resets channel lists for all modules
   SET IPIPE1 B0          // 2nd channel in channel list on module #1
   SET IPIPE2 B1          // 1st channel in channel list on module #2
   SET IPIPE3 B1          // 2nd channel in channel list on module #2
   SET IPIPE4 B2          // 1st channel in channel list on module #3
   SET IPIPE5 B2          // 2nd channel in channel list on module #3
   SET IPIPE6 B3          // 1st channel in channel list on module #4
   SET IPIPE7 B3          // 2nd channel in channel list on module #4
   SET IPIPE8 B4          // 1st channel in channel list on module #5
   SET IPIPE9 B4          // 2nd channel in channel list on module #5
   SET IPIPE10 B5         // 1st channel in channel list on module #6
   SET IPIPE11 B5         // 2nd channel in channel list on module #6
   SET IPIPE12 B6         // 1st channel in channel list on module #7
   SET IPIPE13 B6         // 2nd channel in channel list on module #7
   SET IPIPE14 B7         // 1st channel in channel list on module #8
   SET IPIPE15 B7         // 2nd channel in channel list on module #8
   TIME 10                // sample clock at 10 microseconds, or 160 microseconds per channel
   END

PDEFINE MslProc
   SKIP(IPIPE(0..15), 32, 1, 0, $BINOUT)
   END
```

The address B0 is the scan address and it is selected to return an input channel for the scan address, and thus reading it returns the first channel for the MSXB080 module set as B0. Again, the data returned from the first two passes through the input pipe list is invalid due to the pipeline delays. The SKIP command can be used to take an initial skip

of 32 samples, or two samples for each input pipe, and then transfer data continuously to $BINOUT. The 16 channels are sampled at 6250 Hz per channel.

Example #4 – Fast Sampling with the MSXB080 Module

As described in the Software Configuration section, the scan address should be read at a minimum time interval of 3.0 microseconds. That puts a restriction on the number of inputs a system can have to obtain the maximum sample rate of 333 kHz per channel. Assume the system has one MSXB080 module with the DAPL code as described in Example #1. Most DAP boards have a minimum time interval of 0.6 microsecond for digital inputs. In order to read the scan address B7 at an interval of 3.0 microseconds, we need to have five inputs declared in the input definition. The DAPL code then becomes the following:

```
RESET

IDEFINE MslInputs
  CHANNELS 5
  SET IPIPE0 B7          // 1st channel in channel list, D0, resets scan
  SET IPIPE1 B1          // 2nd channel, D1
  SET IPIPE2 B1          // 3rd channel, D2
  SET IPIPE3 B1          // 4th channel, D3
  SET IPIPE4 B1          // 5th channel, D4
  TIME 0.6               // sample clock at 0.6 microsecond, or 3.0 microseconds per channel
  END

PDEFINE MslProc
  SKIP(IPIPE(0..4), 10, 1, 0, $BINOUT)        // or MERGE(IPIPE0, IPIPE1, IPIPE2, IPIPE3, IPIPE4, $BINOUT)
  END
```

The time between reading two consecutive input pipes can be as small as the minimum time interval for the DAP model, as long as the scan address is read at a minimum interval of 3 microseconds.

This example shows that with a minimum sample time of 0.6 microsecond, most DAP boards can sample five inputs at the maximum rate of 333 kHz with one MSXB080 module. If the DAP board can sample faster, such as the DAP 5216a/627 with a minimum sample time of 0.5 microsecond (or 2.0 MHz), the number of inputs goes up to six with the following input definition:

```
IDEFINE MslInputs
  CHANNELS 6
  SET IPIPE0 B7          // returns 1st channel in channel list, resets scan
  SET IPIPE1 B1          // 2nd channel
  SET IPIPE2 B1          // 3rd channel
  SET IPIPE3 B1          // 4th channel
  SET IPIPE4 B1          // 5th channel
  SET IPIPE5 B1          // 6th channel
  TIME 0.5               // sample clock at 0.5 microsecond, or 3.0 microseconds per channel
  END
```

Example #5 – Mixed Sample Rates with Two MSXB080 Modules

The application requires four channels on one MSXB080 module to be sampled twice as fast as the eight channels on another MSXB080 . The hardware setting of the MSXB080 is similar to that shown in example #2 except for the sampling address.

Module	*Input Address*	*Scan Address*	*Sampling Address*	*Sample Returns Input*
MSXB080 #1	1	7	6	YES
MSXB080 #2	2	7	7	NO

Unlike the settings in example 2, the scan address in this case has to be different from the input addresses. It has its default value of B7. For the module with the fast channels, the sampling address has to be different from the input and scan addresses. It is set to B6 in this example.

Assume that the channel list for MSXB080 #1 has the first four channels D0 to D3 and MSXB080 #2 has all eight D0 to D7. The DAPL configuration for sampling the channels on MSXB080 #1 twice as fast as the ones on MSXB080 #2 is shown below.

```
RESET

IDEFINE MslInput
   CHANNELS 16
   SET IPIPE0 B7          // resets the list, returns D0 on module #1
   SET IPIPE1 B1          // D1 on module #1
   SET IPIPE2 B1          // D2 on module #1
   SET IPIPE3 B1          // D3 on module #1
   SET IPIPE4 B2          // D0 on module #2
   SET IPIPE5 B2          // D1 on module #2
   SET IPIPE6 B2          // D2 on module #2
   SET IPIPE7 B2          // D3 on module #2
   SET IPIPE8 B6          // latches values from last scan and starts acquisition cycle for module #1, returns D0 for #1
   SET IPIPE9 B1          // D1 on module #1
   SET IPIPE10 B1         // D2 on module #1
   SET IPIPE11 B1         // D3 on module #1
   SET IPIPE12 B2         // D4 on module #2
   SET IPIPE13 B2         // D5 on module #2
   SET IPIPE14 B2         // D6 on module #2
   SET IPIPE15 B2         // D7 on module #2
   TIME 10                // sample clock at 10 microseconds, or 160 microseconds per channel
   END

PDEFINE MslProc
   SKIP(IPIPE(0..15), 32, 1, 0, $BINOUT)
   END
```

The sampling addresses for the two modules have to be different because we want the eight channels on the slow module to be read once through the scan. The values for those eight channels are latched when B7 is read at the beginning of the input pipe list and retrieved one-by-one as the DAP reads each input pipe. When the DAP reads B6, which is the sampling address of the fast module, new values are latched only for the fast module and not the slow module. So for each pass through the input pipe list, the DAP gets two values for each channel for the fast module and one value for each channel for the slow module.

The first two passes through the input pipe list do not return any valid data. Going into the third pass, the transition to the scan address B7 latches the values from the last scan and returns the value for D0 from module #1. Since

module #1 is specified to return an input channel for the scan address, it returns the first channel on its channel list when the scan or sampling address is read. The next three reads of B1 return values for D1, D2, and D3. Reading the input address of module #2 four times returns the values for D0 through D3. Then reading the sampling address B6 starts another acquisition and latches values from the last scan to get new data for the four channels on module #1. We do not want to reset the list at this point because the last four channels on module #2 are yet to be read.

The sample rate for the channels read only once through the pass, i.e. the eight channels D0 – D7 on module #2, is 6.25 kHz per channel. For the four channels module #1 that are read twice through each pass, the sample rate is doubled at 12.5 kHz.