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Technical Note TN-204 **Version 1.0**

Technical Product Information for the DAP 3200a™

The DAP 3200a models

- have an Intel i486 processor onboard
- come with 1M or 4M of DRAM onboard memory
- are compatible with other a-Series boards
- work with the PC/AT/ISA bus for 286/386/486 PC or Pentium platforms
- transfer data to PC at high rates — up to 909K samples per second
- allow fast real-time processing
- offer low latency—0.2 ms task time quantum—for fast response
- increase sampling period resolution to 100 ns
- provide onboard emulation of DSP routines
- sample or update the digital section at up to 1.66 million values per second
- sample analog inputs at up to 769K samples per second
- update analog outputs at up to 833K samples per second each
- each have expandable analog and digital inputs/outputs
- comply with the European EMC Directive and are CE marked.

There are four DAP 3200a models: the DAP 3200a/111, the DAP 3200a/214, the DAP 3200a/315, and the DAP 3200a/415. They vary only in memory size and CPU type and speed. This technical note describes the DAP 3200a in terms of its similarities with other a-Series boards, software speed and functionality, and hardware characteristics.

All a-Series boards use the same type of analog and digital connectors, so all of these boards use the same cabling and external boards for termination and expansion. Accessories used with any a-Series Data Acquisition Processor™ can be used with the DAP 3200a.

The onboard multitasking operating system, DAPL™, runs on every Data Acquisition Processor, and ensures that hardware-level differences are transparent. DAPL is a complete software environment for real-time data acquisition. To aid application development, DAPL comes complete with many system diagnostics in addition to automatic memory and system checks that are done at initialization. Tasks that perform averaging, triggering, PID control, fast Fourier transforms, filtering, arithmetic operations, and many other functions are pre-coded in DAPL. These tasks, or DAPL commands, are chained together to form a complete data acquisition application. Custom commands can be written with the Developer's Toolkit for DAPL™ if multiple commands need to be combined, or if a specific application cannot be implemented with standard DAPL commands. On the next page, some standard DAPL commands are tabulated with a comparison of their speed of execution on the DAP 3200a/415 and DAP 2400a™/6.

Another common element among a-Series boards is the bus interface. Like every a-Series Data Acquisition Processor, the DAP 3200a is compatible with the PC/AT/ISA bus for 286/386/486 and Pentium platforms. Dual 1K word BiFIFO buffers allow fast data transfer to and from the host PC. The maximum transfer rates for the DAP 3200a are 909K samples per second to sample and transfer information to the PC, and 957K samples per second to send information from the PC.

The main differences between the DAP 3200a and other a-Series boards is that the DAP 3200a has an onboard Intel i486 processor, and has a faster analog input section. The DAP 3200a is therefore an excellent choice for applications where there is a need for real-time processing of data in the time interval between samples, and for applications requiring fast sample rates. For example, even at maximum analog sampling rates where the sample period is 1.3 microseconds, an i486DX4 CPU running at 96 MHz can execute 125 internal cycles between samples. These 125 internal cycles are allocated for DAPL command processing and DAPL system overhead. Where even faster analog input sampling is needed, the DAP 3400a™ provides essentially four times the sample rate of the DAP 3200a, with an aggregate sample rate of 3.2M samples per second.

The i486 also gives the DAP 3200a low latency: down to a 0.2 ms task time quantum. This means that when low latency mode is enabled, a single task will run for no more than 0.2 ms before DAPL switches to another task. This is crucial for process control applications where data must be r e-sponded to as quickly as possible.

Table 1: Comparison of DAPL command speeds — DAP 2400a/6 and DAP 3200a/415

DAPL Command	Description	Time of Execution[1] on 2400a/6	Time of Execution[1] on 3200a/415
AVERAGE	Averages groups of 16 data points[2]	70.4 µs	0.6 µs
RFILTER	Filters input data with 20 tap filter	9.4 µs	3.1 µs
DAPL Expression: P3 = P1 + P2	Adds two word-length pipe values together	30.8 µs	2.0 µs
INTERP	Interpolates between two vectors	55.8 µs	2.3 µs

From the point of view of DSP-intensive applications, the main difference between the DAP 3200a and the DAP 2400a is that, while the DAP 3200a has an i486 processor, the DAP 2400a has a 80C186XL processor and a DSP coprocessor. The DAP 3200a handles DSP routines with onboard emulation. This may seem less efficient than a dedicated hardware coprocessor, but the DAP 3200a/415 is faster than the hardware coprocessor in all cases. For non-DSP commands, the DAP 3200a is about four to sixteen times faster than the DAP 2400a.

[1] The speed given is an actual application speed for the DAPL task, including sampling, DAPL task-switching and activation, and simulated transfer time. Kernel speeds for the task are actually smaller.

[2] The speed given is for the entire operation on all data points, including system overhead. Contact Microstar Laboratories for task speed.

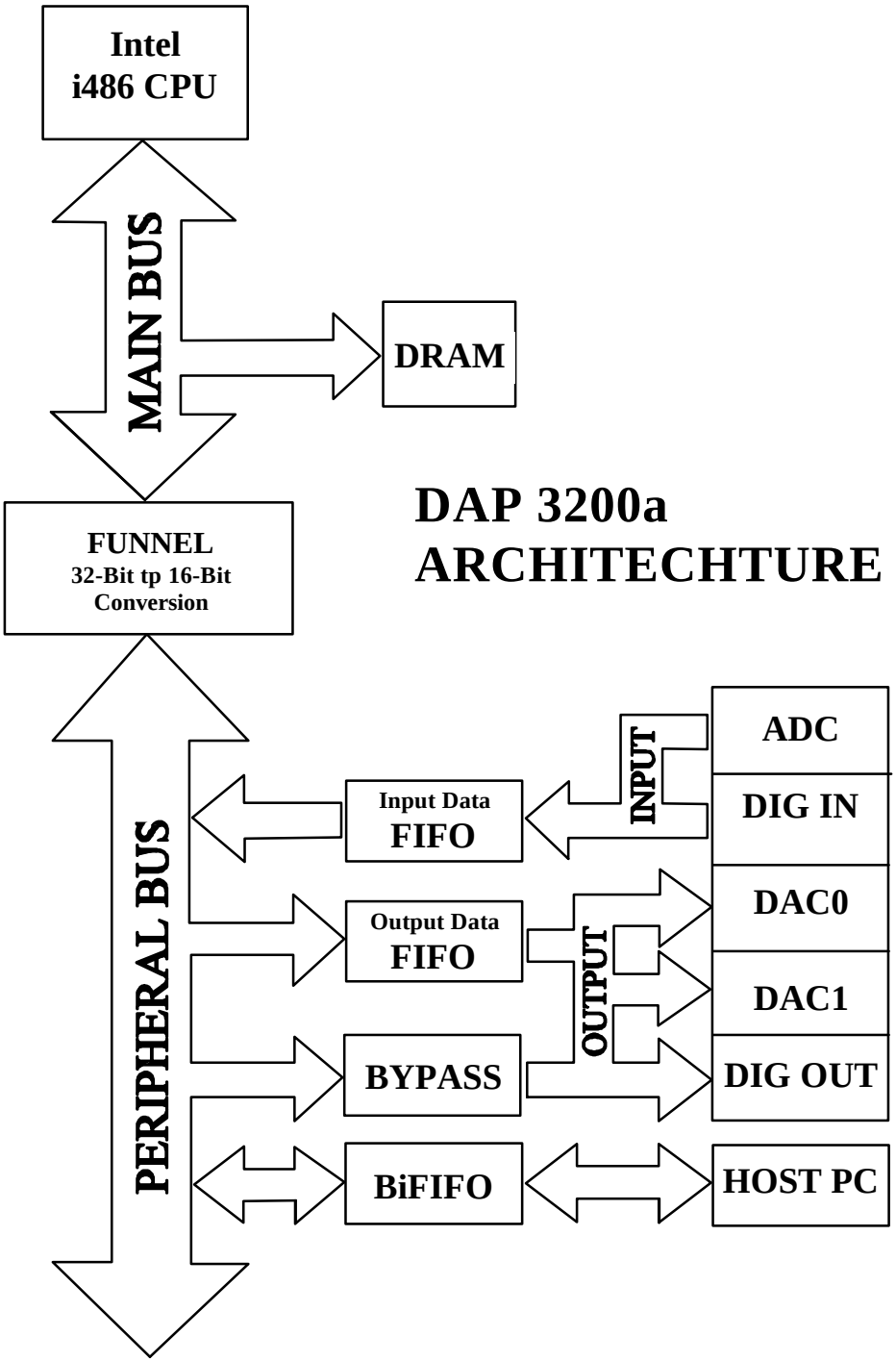

Figure 1: DAP 3200a Data Acquisition Hardware

In addition to high performance processing, the DAP 3200a provides the standard arrangement of complete analog/digital input and output sections. These analog and digital sections are completely expandable — see Table 2 for complete specifications.

Figure 1 displays the architecture of the internal processing hardware of the DAP 3200a. The figure shows the three FIFOs on the DAP 3200a that handle data acquisition and communications. The BiFIFO on the DAP 3200a handles communications between the board and the PC. Information can

be sent in both directions simultaneously, and can be DAPL files, binary or text data, error messages, or DAPL system commands. In addition to the BiFIFO for communications, there is an output data FIFO and an input data FIFO. The data FIFOs are unidirectional, buffering data for input and output.

Data are acquired or updated via dedicated hardware clocking circuitry at a rate of up to 1.66 million samples per second. Acquisition is clocked at a sampling rate or output rate controlled in software, and the rate is accurately maintained by onboard crystal-controlled timers. The sample period is specified with a resolution of 100 nanoseconds and the sample rate is accurate to 50 parts per million.

In addition to onboard timing, the DAP 3200a also has provisions for external triggering and clocking for the input and output sections.

The 16-bit digital input port and the analog-to-digital converter are attached to the Input Data FIFO, one of the unidirectional data FIFOs. The maximum aggregate sample rate is 1.66M samples per second. Digital input alone can run at up to 1.66M samples per second. The maximum analog input sample rate is 769K samples per second.

The digital output port and the two analog outputs are attached to the Output Data FIFO. The max i-mum aggregate update rate is 1.66M updates per second. Digital output alone, like digital input, can run at up to 1.66M updates per second. Each of the analog outputs can be updated at 833K updates per second.

The i486 processor bus on the DAP 3200a gives a maximum bandwidth of 2M words—or samples—per second of input/output for data. An example of using this maximum bandwidth is a situation where both input sampling and output updating occur. In this example, two channels of digital data and one channel of analog data could be acquired at 330K samples per second, the digital port could be updated at a rate of 330K updates per second, and two analog outputs could each be updated at a rate of 330K updates per second. Other mixes of sampling and update rates may be used, as long as the total throughput for input or output does not exceed 2M words per second.

The Bypass section shown in Figure 1 allows the 486 processor to asynchronously update either the digital or analog outputs. This means that periodic timing is not guaranteed, rather the 486 processor will attempt to update the outputs whenever a time slice for this task becomes available. This is useful in control application where a digital output, for example, needs to open or close a valve at irregular intervals.

In addition to the processor and data transfer hardware, some important hardware specifications of the DAP 3200a are provided in Table 2.

Table 2: DAP 3200a Typical Hardware Specifications

Specification	DAP 3200a/111	DAP 3200a/214	DAP 3200a/315	DAP 3200a/415
Dimensions	13.33" x 4.8"	13.33" x 4.8"	13.33" x 4.8"	13.33" x 4.8"
Weight	12.8 oz	12.8 oz	12.8 oz	13.3 oz
CPU type	Intel 80486SX	Intel 80486SX2	Intel 80486DX2	Intel 80486DX4
CPU clock speed	24 MHz	48 MHz	64 MHz	96 MHz
CPU DRAM	1 Mbyte	4 Mbytes	4 Mbytes	4 Mbytes
Bus support	ISA AT	ISA AT	ISA AT	ISA AT
PC interface hardware	dual 1 KWord BiFIFO buffers	dual 1 KWord BiFIFO buffers	dual 1 KWord BiFIFO buffers	dual 1 KWord BiFIFO buffers
PC transfer mode	I/O Interrupt	I/O Interrupt	I/O Interrupt	I/O Interrupt
Maximum transfer rate	833K samples/sec	833K samples/sec	909K samples/sec	909K samples/sec
Power requirements	+5V, 3.0 Amps	+5V, 3.0 Amps	+5V, 3.0 Amps	+5V, 3.0 Amps
Operating temperature	0-50 °C	0-50 °C	0-50 °C	0-50 °C
Accuracy of crystal clocks	50 parts per million	50 parts per million	50 parts per million	50 parts per million
Type of A⇒D converter	Successive Ap-proximation	Successive Ap-proximation	Successive Ap-proximation	Successive Ap-proximation
Model of A⇒D converter	Burr-Brown ADS7819	Burr-Brown ADS7819	Burr-Brown ADS7819	Burr-Brown ADS7819
Max. analog sampling at Gain = 1 Gain = 10 Gain = 100 Gain = 500	 769 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s	 769 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s	 769 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s	 769 K samples/s 125 K samples/s 25 K samples/s 2 K samples/s
Number of analog channels	16	16	16	16
Expandable To	512	512	512	512
Input voltage ranges	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V
Resolution -5 to 5 V range	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy -5 to 5 range	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV	±1 LSB ±2.4 mV
Non-linearity	0.05%	0.05%	0.05%	0.05%
Input bias current	12 nA	12 nA	12 nA	12 nA
Analog input impedance	>> 10 MΩ	>> 10 MΩ	>> 10 MΩ	>> 10 MΩ
Common mode rejection	90 dB	90 dB	90 dB	90 dB
Type of D⇒A converter	Voltage Output	Voltage Output	Voltage Output	Voltage Output
Model of D⇒A converter	Analog Devices AD767	Analog Devices AD767	Analog Devices AD767	Analog Devices AD767
Maximum analog update rate[3]	833K updates/sec	833K updates/sec	833K updates/sec	833K updates/sec
Max. input voltage (fault-protected multiplexers)	±25 V	±25 V	±25 V	±25 V

[3] The DAP 3200a can update each of its two standard analog outputs independently at 833K updates per second. When analog output expansion is used, the update rate for expanded channels is determined by the maximum update rate of the digital port.

Expanded Analog Output Rate = 1.6M / (4 * Number of Channels)

Table 2: DAP 3200a Typical Hardware Specifications, continued

Specification	DAP 3200a/111	DAP 3200a/214	DAP 3200a/315	DAP 3200a/415
Number of output channels	2	2	2	2
Expandable to	66	66	66	66
Output ranges	0 to 5 V -2.5 to 2.5 V - 5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V	0 to 5 V -2.5 to 2.5 V -5 to 5 V -10 to 10 V
Resolution -5 to 5 V range	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV	12 bits 2.4 mV
Accuracy -5 to 5 V range	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV	±1 LSB, ±2.4 mV
Analog output signal to noise ratio	0.0002% of full scale	0.0002% of full scale	0.0002% of full scale	0.0002% of full scale
Output impedance	0.05 Ω	0.05 Ω	0.05 Ω	0.05 Ω
Current source maximum	±1 mA	±1 mA	±1 mA	±1 mA
Digital output logic	ACT TTL	ACT TTL	ACT TTL	ACT TTL
Digital input logic	FCT TTL	FCT TTL	FCT TTL	FCT TTL
Maximum digital update rate[4]	2M words/sec	2M words/sec	2M words/sec	2M words/sec
Number of input bits Number of output bits	16 16	16 16	16 16	16 16
Expandable to	128 input bits and 1024 output bits	128 input bits and 1024 output bits	128 input bits and 1024 output bits	128 input bits and 1024 output bits
Digital input Min. logical high Max. logical low Max. current sink Max. current source	 2 V 0.8 V 5 µA 5 µA	 2 V 0.8 V 5 µA 5 µA	 2 V 0.8 V 5 µA 5 µA	 2 V 0.8 V 5 µA 5 µA
Digital output Min. logical high Max. logical low Max. current sink Max. current source	 2.4 V 0.5 V 12 mA 15 mA	 2.4 V 0.5 V 12 mA 15 mA	 2.4 V 0.5 V 12 mA 15 mA	 2.4 V 0.5 V 12 mA 15 mA
External clock input min. pulse width	25 ns	25 ns	25 ns	25 ns
External trig. input min. pulse width	60 ns	60 ns	60 ns	60 ns
Trigger modes	GATED ONE-SHOT	GATED ONE-SHOT	GATED ONE-SHOT	GATED ONE-SHOT

[4] This figure is the maximum throughput of simultaneous digital input and output. Either digital input or digital output operating alone can maintain a throughput of 1.6 M words/sec.